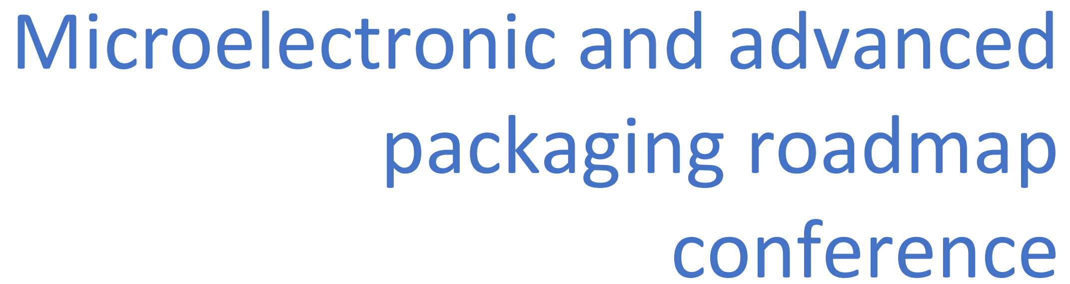

Microelectronic and advanced packaging roadmap conference

August 14 & 15, Arlington, VA

Summary Report

Introduction

Microelectronics and Advanced Packaging Technologies (MAPT) is a critical multidisciplinary field with the potential to transform the design and manufacture of future microchips. These advances build upon breakthroughs in advanced packaging, 3D monolithic and 2.5D/3D heterogeneous integration (HI), electronic design automation, nanoscale manufacturing, new materials, and energy-efficient computing.

A critical contribution of the MAPT road mapping effort is to assure future design, development, and manufacturing of heterogeneously integrated chips in the U.S. The MAPT Technical Committee has identified the key drivers of MAPT innovation and begun planning research in these areas. Advanced packaging is key to meeting the needs in these areas; the limits of transistor scaling will require assembling separately manufactured components, called chiplets, to create advanced Systems in Package or SiPs.

The main goal of the conference was to unveil the Microelectronic and Advanced Packaging Technologies Roadmap – an industry-wide initiative of major impact on the semiconductor and ICT industry, which will drive public-private research investments in support of the CHIPS Act. The conference celebrated the first 3D semiconductor roadmap to guide the forthcoming microelectronic revolution, like the International Technology Roadmap for Semiconductors (ITRS) has served in the past.

This conference was intended to stimulate collaborative effort 'from materials to system' aiming at establishing revolutionary paradigms to support future sustainable manufacturing of energy-efficient chips for the vast range of future workloads.

The 2-day conference was constructed to include selected overview presentations and panel discussions. It encouraged and enabled interactions by allotting sufficient time for in-depth panel-participant interactions after each session. In each session, participants were asked to identify potential research topics that would enable the transfer of new ideas to the synthesis of systems whose performance cannot be derived from conventional semiconductor technologies. Successful execution of the conference goal is now used to guide the development of future R&D programs in microelectronic manufacturing. The output of this conference will guide the future developments of the MAPT Roadmap and support the CHIPs Act by reflecting an informed view on key scientific and technical challenges related to future chipmaking including advanced packaging, based on new quantitative analyses and projections.

Session 1: Advanced Packaging

Moderator: Muhannad Bakir / Georgia Tech
Keynote: Griselda Bonilla / IBM

Panel consisted of: Charles Woychik / Skywater Technologies; Henning Braunisch / Intel; Shelby F. Nelson / Mosaic Microsystems; Babu Mandava / 3D Glass Solutions; Griselda Bonilla / IBM; George Orji / CHIPS R&D Office

Questions for the Panel:

1. Which are the packaging technologies that the US should focus on and how can we ever reclaim leadership in advanced packaging?
   - What are barriers and what are the payoff in terms of the drivers (performance, energy, functionality etc.)?
   - Will these technologies ensure we leap ahead everyone else?

The panel agreed that heterogeneous integration will be a key enabler to continue scaling of performance, energy, cost, and form factor. No particular packaging technology was identified as the "key" enabler. Rather, the panel believes a multitude of advanced packaging options will be needed as function of application and market. Among these options are interposers, bridge-chip, 3D stacking, and glass packaging.

The panel was also asked if it was appropriate for the US to invest into known technologies (hybrid bonding or bridge-chip) or if we should focus on 'future' and more differentiated technologies. The panel seemed to agree that even if these are known concepts, there is value in creating the complete ecosystem and facilities in the US so long the ideas are still of value. This prompted questions from the audience regarding how to balance "catching-up with the rest of the world" vs. "leap ahead."

The audience also asked about reliability and understanding failure analysis in advanced 3DHI. The number of new materials and interfaces in such systems is large and require very careful understanding.

2. 3DHI is application driven: sensing, communication, edge AI, data center etc. What are the challenges to integration of mm-wave, photonics, sensors, and high-voltage devices/chiplets in 3DHI and how will the technologies we just discussed help us here?

mm-wave and photonic applications have very unique demands that complicate 3DHI. For example, photonic devices are temperature sensitive and require unique thermal isolation and control strategies. Alignment is also challenging, especially for fiber attach. For mm-wave, it was noted that glass packages in some applications provide significant performance benefits due to material properties relative to silicon. There was some concern on the use of glass for automotive or other harsh environments.

There was extensive discussion on whether glass wafers or glass panels will be the key to the success of glass-packaging technology. The conclusion is that it all depends on the substrate size needs; if large glass packages are needed, then glass panels will be key and glass panel processing is very different from that of glass wafers.

3. How can we better engage Universities to help solve challenges?

    - Given the cost of the tools, space, and staff needed to have advanced HI research in academia, should we pursue central research nodes vs. distributing over a large number of schools.
    - How can we create better pipelines from lab-to-fab in advanced packaging?

Clearly, research, education, and workforce development (WFD) are key. There is a need for new advanced packaging courses across the country. These courses should give students hands-on experience with advanced packaging tools that not only cover fabrication but also assembly and bond. However, this is also very challenging to implement, especially at scale. The cost of advanced packaging tools (assembly and bonding) is quite large, with some tools in the $5 - $10M range, which does not include ongoing operating costs. Further, for these tools to have the latest/greatest capabilities, they are generally geared towards very large substrate sizes, making not only the footprint of such tools very large but also requiring large substrates to process, which is cost prohibitive for a university setting. So, it is not clear that many universities would be able and interested in supporting such capabilities. One of the panelists suggested there is a need for a national 3DHI facility that acts like a sandbox – giving users ultimate flexibility in the testing and exploring innovative ideas. Such a sandbox facility could be open to or affiliated with universities.

At this point in the session, we were nearing the end of the hour. The audience was very active and asked many questions, some of which were incorporated into the discussion above. A common theme from the Q&A:

- How do we leap head? What comes after CPU/GPU-HBM integration?
- What are the issues in thermomechanical reliability and how can one better predict failures?
- What are the needs of systems for sensing and actuation?
- How long will the chiplet era last and what is life after chiplets?

Session 2. Microelectronics Workforce Development

Moderator: Kashyap Yellai / SRC
Keynote: Doreen Edwards / RIT

Panel consisted of: Doreen Edwards / RIT, Shari Liss / SEMI, Shyam Aravamudhan / N.C A&TSU, Katy Crist/TEL, John Goodenough / U Sheffield, Quinn Spadola / NNCO

It is a unanimous voice among panelists and attendees across industry, government, and academia that addressing the workforce (talent) shortage in the next 5 to 10 years is of the utmost priority. While winning the hearts and minds of K–12 students is crucial to sustaining the long-term flow of talent into the semiconductor field, a higher priority is attracting and incentivizing the current generation of community college and 4-year undergraduate students to graduate with STEM disciplines of relevance to the semiconductor industry to close the diverging gap of talent supply shortage.

In addition to 8–10-week semiconductor-sponsored internship programs, students from co-op universities such as RIT should be considered for industry-developed internship opportunities. Alternative earn-to-learn programs to incentivize 2-year and 4-year college students should also be considered to lower the cost of college education and foster a design and technology mindset.

Universities are not currently incentivized to prepare students for recruitment, and the industry alone cannot address this challenge. Government funding is key to developing these programs and will play a vital role in fixing the leaky pipeline. CHIPS Act funding presents a once-in-a-lifetime opportunity, and every effort should be made to leverage the funds and provide direction to the government for optimal appropriations.

The talent shortage challenge can only be addressed through collaborative efforts, and it should certainly involve a public-private partnership (PPP). Understanding existing organizations and investing in programs with a proven track record and the potential to provide solutions at a national scale will be a critical step in execution. Tensions between operating organizations should be minimized to facilitate progress toward our a collective goals. The average age of employees in the semiconductor industry, which currently stands at 57 years, needs tomust be lowered. The industry should be prepared to onboard employees and be transparent about pay. Industry input on knowledge, skills, and abilities, or KSAs, is vital for guiding universities in curriculum development and training.

In addition to the issue of students in the pipeline, there is also a shortage of instructors. Teaching STEM degree programs is challenging and retaining students for 4-year colleges is even more difficult. Government-aided tutoring or teach-the-teacher programs offer a smart alternative to help students graduate with STEM majors.

Some follow-up thoughts / actions include:

1) How can we influence the influencers (TikTok, Instagram, etc.) to talk about semiconductors? A Netflix show/series would be great…

2) A software hardware co-design engineering job role needs to be developed. The KSAs for this role are not completely understood, but it presents an opportunity to start the conversation.

3) In WFD discussions, we are missing the voice of the students as we are only anticipating what students want. We should seek way to obtain student's involvement and feedback.

4) Educational 'silos' will not meet the needs of the industry or the nation.

5) Missing Millions – how to support those who don't have family or other "incentives" to go into microelectronics?

Session 3: Sustainability & Energy Efficiency

Moderator: James Ang / PNNL
Keynote: Brook Tvermoes / IBM

Panel consisted of: Matt Marinella / ASU, Katherine Hutchison / EMD Electronics, Sadas Shankar / SLAC National Laboratory, Austin Rovinski / NYU, David Speed / GlobalFoundries, Brook Tvermoes / IBM

The main discussion points/findings included:

Energy Efficiency

- There has been 50+ years of progress in energy per useful computation. The slowing/end of Moore's Law means we are approaching the limits of what can be economically achieved with digital CMOS. This together with increasing proliferation of computing devices and need for computing, are the drivers for the Decadal Plan seismic shift #5, highlighting the need to discover computing

paradigms/architectures with a radically new computing and communication trajectory demonstrating >1,000,000x improvement in energy efficiency. This is a key concern for the future, as computing is forecast to consume a significant and growing fraction of the future global electricity production.

- This motivates R&D in other processor devices and architectures including analog, neuromorphic, and quantum. These emerging technologies have a critical role to play in energy efficiency. Most energy for computation is expended from moving data, thus the importance of breakthroughs in advanced packaging that support tighter integration of interconnect technologies, optical interconnects, and advanced memory interfaces, are needed.
- Hardware-software co-design to develop domain-specific accelerators, that are packaged with commodity processor cores to create specialized heterogeneous computing will be important opportunities for energy efficiency. Co-design will concurrently develop the applications, algorithms, and the supporting software stack that will map to domain-specific accelerators and commodity processors; and memory advances to support energy efficient heterogeneous computing concepts.

Environmental Sustainability

- Characterizing the environmental impact of microelectronics from end to end is complex and multifaceted.
- There are several challenges that the industry needs to address to decrease the environmental impact of microelectronics including challenges associated with:
    - Energy efficiency, resource conservation and waste minimization
    - Developing more benign chemistries, finding alternatives to rare earth metals and minimizing environmental releases;
    - Developing more circular pathways to enhance the recovery and reuse of valuable materials and chemicals;
    - Developing a common set of environmental metrics and data standards, that cover the entire lifecycle of microelectronics, to facilitate consistent measurement and reporting of the industries' environmental performance, enable tracking of the industry's progress over time and enable industry to better understand the potential environmental impact of design choices for new technologies.
- Brooke's Keynote highlighted significant differences in greenhouse gas (GHG) emissions during lifetime usage versus manufacturing/production based on semiconductor product type. GHG emissions and energy usage metrics also track the complex interactions that impact the sustainability of microelectronics fabrication as fab processes transition to Extreme Ultraviolet (EUV) Lithography. It is also important to keep in mind that the semiconductor industry's environmental challenges extend well beyond just GHG emissions and energy efficiency, and encompass crucial issues such as natural resource conservation, including water conservation. Chemical-Mechanical Planarization (CMP) is one of the largest producers of wastewater and the use of ultra-pure water is expected to increase as the complexity of the nodes continues to increase driving higher number of CMP and wet (etch, clean, etc.) steps. There is also a need to develop more efficient recovery and purification processes to increase the reuse of water.
- One of the biggest sustainability challenges for microelectronics fabrication is to: a) inform the selection of new materials and processes, and b) incorporate them into manufacturing processes that have minimal impacts on the environment.
    - Our longstanding goal is to select the most benign materials that are effective for a process, and then to use a combination of controls, recycling/treatment technology to assure that the environmental impacts of fab emissions and wastes are minimal.

- One of the challenges in doing so, is often with obtaining the information needed to make fully informed selections. There is not always good or complete information available on the physical chemical properties of a chemical or how it behaves in the environment or biodegrades.
- Another big challenge is getting the industry to adopt environmentally friendly processes, materials, and abatement systems, especially at existing fabs. There needs to be a compelling sustainability and financial impact to overcome the yield risk of changing a process. Despite the potential cost and impact on yield, existing fabs need to move away from using materials based on perfluoro alkyl substances (PFAS).
- There is an immediate need for a focused semiconductor industry effort to optimize and minimize PFAS use in processes where PFAS are essential; to evaluate and move to non-PFAS alternatives where feasible, and to develop and validate controls and abatement technologies to prevent environmental releases for uses where there are no currently known viable alternatives. Identifying safer alternatives with the same performance characteristics as PFAS will be extremely challenging and given the multiple properties that PFAS incorporate, it is unlikely there will be a universal replacement for PFAS but likely a combination of specific solutions.
- Leading edge fabs have the opportunity to build sustainability into the initial design, especially ways to minimize water and energy consumption. The leading-edge IDMs/foundries seem to be more open to new options that make their processes sustainable. For example, we are seeing multiple requests for etch gases with lower Global Warming Potential (GWP) to replace established high GWP etch gases. It may also be possible to design new fabs to consider PFAS-free alternatives during the planning stage.
- R&D over the past 40+ years has driven important improvements in chemical prediction methods. The combination of quantum chemical methods and AI, for instance is yielding good improvements, but it is important to recognize that significant advancements in these methods is still needed. For example, the accuracy of current best methods using quantum with AI for predicting biodegradability remains very low, with important groups of chemicals not yet evaluated.
- A second big challenge is the amount of e-waste our industry creates – *how can we handle E-waste when we can't even handle plastic waste?* According to the International Waste Electrical and Electronic Equipment forum, 5.3B cell phones were thrown away in 2022. Overall, nearly 60M tons of e-waste was disposed and less than 20% was recycled last year. We need to design our electronics systems to be more easily recycled. For example, Jiva Materials offers PCB created with natural fibers encased in non-toxic polymer which can be dissolved in hot water. This allows the components to be separated from the board intact instead of the typical shredding process.
- We need to become 100% circular industry. Developing more circular pathways and improving the extraction efficiency of rare earth elements may also build supply chain resilience by enabling the reuse of rare earth elements.

Session 4: Foundational Microelectronics Layers of MAPT

Moderator: Kanad Ghose / Binghamton U
Keynote: David Robertson / Analog Devices

Panel consisted of: Tayseer Mahdi / Intel; Michael Spencer / Morgan State; Mary Ann Maher / Softmems; Thomas LeBrun / NIST; Min Tsao / Siemens EDA

Processing heterogeneity. The semiconductor field has run through several phases of advancing performance - though the 90's and early 2000s, progress was measured in increasing performance of a handful of core building blocks—including microprocessors, DRAM/SRAM memory, etc. Through the 2010's, many advances were achieved through parallelism—distributing workloads/functionality across an array of standard building blocks. Today (and going forward), there is a far greater emphasis on exploiting a variety of optimized elements, i.e., specialized accelerators to augment the processing that was done by general-purpose processing chiplets. This means going beyond x86 type microprocessors to GPUs, TPUs, compute-in-memory architectures, analog processing and more. Fine line CMOS processes are still the focus of much development, but process variants are proliferating to provide effective solutions to different requirements: BCDMOS, SiGe, GaN, GaAs, SiC. Advances in heterogenous integration will allow this diversity to be integrated in near-monolithic form factors. This over-arching trend also enables several sub-trends.

Sensor explosion. Ubiquitous computing and IoTs are fueling an appetite for ubiquitous, multi-mode sensors, and a significant portion of these sensors will be solid state. Sensors frequently are based on very different fabrication processes. The world of sensors is at the forefront of using heterogeneous integration. Everything is truly heterogeneous in nature – the sensors, the electronics for control and signal processing, storage etc. frequently are based on very different fabrication processes. Packaging does remain a challenge with sensors/MEMS that have to remain exposed. Cost – delivering low-cost solutions – is also a challenge. In general, ensuring reliability is a very important consideration for applications like automotive and critical wearable/implanted health monitoring systems. Test is also a significant challenge, since sensor and actuator ICs often create unique requirements for lab characterization as well as production test. New sensors incorporated into clothing are but one example requiring standards and tests for washability. Printed electronics certainly has a role for sensors- in addition for wearables a rigid MEMS chip may be combined with printed interconnect. The industry is already using flexible substrates in some applications and this will continue. Availability of material properties in multiple energy domains and material characterization under bending and stretching will be important for flexible sensor realization.

Analog Renaissance. Exponential acceleration in the number of deployed sensors feeding the endless appetite for data creates a potential "deluge" of information. It is impractical (in terms of power and cost) to digitize all of this in raw form and route it to central processing, so there will be a growing demand for "processing at the edge" and "analog pre-processing" to achieve 2 to 4 orders of magnitude of dimensionality reduction in the data. Analog processing does not replace existing digital processing, but it will be critical in pre-processing at the edge. Analog processing is specific domains, where some approximations are allowed, will offer significantly higher energy efficiencies. An example of this will be emergent analog AI accelerators and chiplets for neuromorphic processing.

Power Conversion for SiPs. Innovations will be driven by the extremes: large, massively integrated systems (like high performance compute in data centers), extremely high voltage/high current systems involved in "smart grid" power routing, EV battery systems etc., and "nano-power" tiny form factor systems for IOT deployments. Since many of these issues come down to fundamental physics, there will be a big emphasis on further development of new materials, processes, and devices (SiC, GaN, piezo electrics). For high power delivery, distributed/embedded voltage converter chiplets functionality inside the package will be the way to go. Cooling needs to be directed to the power devices. GaN devices will be the best to use here. For the EV market, new generations of SiC and GaN both have a role. For energy scavenging, single crystal GaN based piezoelectric generators look promising. Materials innovations need to continue in this segment. This is also true for passives in the power conversion chiplets to support small sizes. Heterogenous integration places big demands on efficiently moving multiple power domains

into tight spaces—architectural techniques like backside power delivery will continue to attract a lot of attention.

Thermal management. 3D integration exaggerates this challenge, since traditionally the “z-axis” in ICs has been exploited for thermal routing. Thermal management for medium to high power 3D chiplet stacks remains an open challenge. In general, the thermal challenge is being exacerbated as SiPs with 300 Watts to upwards of 1000 Watts. There is also the added problem of hot spots introduced by in-package regulators/converters. Liquid cooling solutions for the package, both single and two-phase will play a key role here.

Sustainability (and the path to 1000x power reduction). This will require more than circuit or process improvement—the whole system will need to be re-architected. The answer lies in using alternative processing paradigms, processing data where they are stored or acquired. Analog memory with embedded processing is an example as are processing chiplets near memory chiplets. Circuit or device improvements offer factors of 2x-4x improvement. Radical improvements call for re-architecting the system itself to process only on demand. The scope is very wide and well will need all solutions to come together to realize the 1000X goal.

Photonics. Photonics has traditionally played a narrow (though critically important) role in the semiconductor/information/communications technology ecosystem—including imaging and highly efficient data transport over distances. The proliferation of sensors is expanding that dimension (including Lidar ranging and a variety of optically based chemical and gas sensors), and the advantages of optical data transport are making their way into shorter distance applications. Co-packed photonics has been demonstrated as a viable technology to use in high-end HI systems for communications. Metrology and measurement standards are very important for the photonics world. There are some recent developments in plasmonics for chiplet interconnection. Photonics is playing a role in many types of quantum systems.

Next generation EDA. Multi-domain EDA tools are essential in managing the massive complexity and co-optimization of SiPs. The industry is developing tools for this and AI techniques are being used judiciously where they make sense. The full-stack co-design tool is still not there but a lot of progress has been made. Physics-based modeling is seeing increased use here. Standards are very much needed, but we do need more. EDA support for testing HI systems and run-time monitoring are critical. (Audience:) We do need standards for 3D—for the EDA tools/models and PDKs, for the chip-to-chip interconnectivity (not just for signals, but for power), and for the different substrate technologies. We can reflect on all the elements that had to come together in the 1990’s for the foundry ecosystem to flourish

Patterning for device and interconnect fabrication. Photolithography using extreme UV (EUV) is already being used, high NA EUV is on its way to market and what’s next is hyper NA EUV. We have strong players in the industry to take care of the hardware. Research is a must in the resist and mask space. Resists are getting much thinner, can they be used as etch transfer layers, can metal oxides be used here, what are stochastics impact on thin resists, is there a negative tone and positive tone capability. ML is also crucial to narrow down the molecule library, what functional groups are critical to meet the resolution needs There are revolutionary techniques Directed Self-assembly (DSA) and multi-patterning litho-etch-litho-etch that are complementary techniques to enable fine-pitched patterning.

Session 5: MAPT Systems: Specs, Applications and Security

Moderator: Rafic Makki / Mubadala
Keynote: Ameen Akel / Micron

Panel consisted of: Gamal Refai-Ahmed / AMD, David Gundlach / NIST, Farimah Farahmandi / U Florida, Matt Klusas / Amazon, Ameen Akel / Micron

Session Goals

The session was organized to discuss the impact of a wide variety of application domains and their influence on the direction of key enabling technologies covered by the MAPT roadmap, such as e.g. data center and HPC, mobile, automotive, biomedical, security and privacy, and others.

Keynote main points

The keynote covered the following points:

- History of inflection points in computing, where ground-breaking use cases become popular once compute power enable them.
- AI as an example:
  - Evolved based on the technologies available, but many paths forward possible.
  - Would not have been possible without GPU architectures, increased transistor density, and increased memory bandwidth.
- MAPT must be directed and evaluated end-to-end (i.e., system and application driven).
  - Specialization and domain-specificity will drive future advances.
  - It is no longer possible for each technology to be driven in isolation.
  - Hardware/software co-design is a natural reality and requirement.
  - How do MAPT technologies fit together to tell this story?
- What are the next inflection points, and why are they only possible now? XR, AI, bio-applications, etc.
  - Better energy efficiency; smaller form factors
  - Increased interconnectivity between elements (e.g., chiplets, memory, communications, biocompatibility, etc.)
- Why and how will each of these change the world: improved quality of life, additional security concerns, etc.

Areas of Discussion

- 2040 Vision & Challenges
- Enablement: Policies/Funding
- Application Drivers & Infrastructure
- Security

Panel Discussion

- Much of the discussion centered around what could be missing from the roadmap. An interesting back and forth among the panelists on whether the roadmap is sufficiently focusing on the security aspects required of emerging applications.
- There was also a healthy debate around a vision for the future. Some argued that the roadmap needs to articulate a clearer vision for the future in terms of applications. The major points of the discussion included:

    - Historically, semiconductor technology drove the grandest of applications like the internet, the smart phone, rapid DNA sequencing and so forth. However, we may have reached a time where applications may need to influence the roadmap of semiconductor technology.
    - Others argued that the semiconductor industry cannot play the role of futurists and thus we should focus on technology independent of applications.
- Some panelists voiced concern that the roadmap needs to identify research pathways beyond chiplets and heterogeneous integration to meet the demands of the future applications.
- There was some discussion on whether technology drives applications or applications drive technology. In the end, it is a combination of technology enabling new applications AND applications drivers with special note that applications are the "window" through which most people see microelectronics.
- There was a brief discussion on workforce development and workforce shortages.

Three major takeaways

- While no one can predict the future in terms of novel disruptive applications, current application trends such as autonomous vehicles, generative AI, and electrification will require continuous and major advances in semiconductor technology on all fronts from novel architectures to devices to process technologies.
- Security will continue to take center stage.
- The CHIP act is a great start, but the semiconductor industry will need the continued support of the government, especially on the domestic manufacturing front in order to realize lasting success.

Session 6. MAPT Ecosystem

Moderator: David Henshall / SRC
Keynote: Katie Yu / NXP

Panel consisted of: Mitchell Heins / Synopsys; Elisa Alonso / US Geological Survey; Alain Diebold / SUNY Poly; Kris Bertness / NIST; Erik Hadland / SIA

Session 6 of the MAPT Roadmap Conference discussed the MAPT Ecosystem and specifically included topics from the Roadmap chapters for i) Materials, Substrates, and Supply Chain, ii) Design, Modeling, Test and Standards, and iii) Manufacturing and Process Development Metrology. This was an evolution of the conversation from Session 5 which highlighted Systems Specs, Applications, and Security while serving as a segue into the final conference session, which followed, on the topic of how to move forward after the Roadmap is complete and published.

Kicking off this session, Dr. Katie Yu, Sr. Director, Automotive Processors & Packaging Design from NXP, provided a keynote with insights about navigating technology economics and other characteristics for market growth. This included a review of the complexities of the markets with different applications each having a span of requirements for cost, volume, performance, and energy efficiency. Emerging applications can be thought of as bringing us a smarter world by having smart devices, smart homes and factories, and smart transportation. This smarter world serves as a world machine interface for sensing, perceiving, and reasoning the world to better serve society.

Supporting these emerging smart applications is a complex supply chain that crosses many geographic borders and varies for different products. These border crossings lead to insecurities in the supply chain which lead to economic vulnerabilities. These insecurities are further stressed by the rapidly increasing number of devices and the growth of the complexity of systems. To respond to this, the industry is moving towards chiplets, improved industry standards, and more comprehensive modeling. The supply chain resiliency is supported by moving from a fully global supply chain towards an 'allied' supply chain and ultimately to a regionalized supply chain but at increasing costs. To maintain cost competitiveness and enable edge application performance differentiation through reuse of high performance compute technology, paths to deliver significant cost reduction are needed. As this supply chain resiliency is improving there's a need to also consider environmental sustainability.

The keynote was followed by an esteemed panel discussing different perspectives of the ecosystem. A few highlighted questions were presented to the panel, and thoughtful answers were provided. Below are three thematic sets of questions and their corresponding discussions:

1. How can we start early in the engineering and design processes to make supply chains more resilient and minimize dependencies on critical materials? How can environmental sustainability be considered?
    a. Start considering critical materials early in the R&D cycle, which is typically not done today.
    b. Also consider environmental impact in early stages of R&D so it can be designed into the solution instead of waiting until after a technology is developed and trying to figure out how to scale it sustainably.
    c. Consider the extraction of all critical materials from raw materials, even if they're not the targeted material. The example of Ga extraction from Bauxite used for Aluminum production was given to illustrate this need.
2. What economic incentives can be provided to prioritize working on gaps? What investments can protect economic sustainability/ security? What investments can fill the gap between research and adoption?
    a. Many answers looked to the government to fund the gaps where there is a high financial risk or where there's limited favorable economics for industry.
    b. There was agreement that investors should make more investments in hardware technology.
3. What metrology challenges need to be addressed and how can NIST and National Labs support this?
    a. Moving metrology from the lab and into in-line testing in the fab is an ongoing trend.
    b. There's an industry-wide need to reduce the cost and increase the speed of measurement and test, while also speeding it up so it can be in-line.
    c. Government resources at national labs can help develop techniques for making testing faster, cheaper, and more reliable through automation, application of AI, and through other improvements.

The session was concluded by each of the panelists providing departing thoughts for the audience to consider.

Session 7: Executive Roundtable. MAPT Roadmap: Moving Forward

Moderator: George White / Georgia Tech
Keynote: Jim Wieser / Texas Instruments

Panel consisted of: Yugyun Shin / Samsung, Krystyn Van Vliet / Cornell U., Ajit Manocha / SEMI, Gabriela Cruz Thompson / Intel, Gamal Refai-Ahmed / AMD, Jay Lewis / NSTC

The Executive Leadership panel represented a diverse executive group of stakeholders from industry, government, academia, and non-profit (industry association).

The keynote talk, "Now What", given by Jim Wieser of Texas Instruments set the tone for a robust question and answer session as panelists answered questions while sharing their views on priority areas using the MAPT roadmap as a blueprint.

There were a number of key take aways from the panel included the following:

1) An overwhelming consensus that Education and Workforce Development (EWD) serves as the highest priority as each panelist expressed support for EWD efforts across all stakeholder groups. Workforce requires no IP framework, or other complicated collaboration documentation and should be embraced immediately. Companies should have a good idea regarding specific attributes, skills and qualities in their workforce and convey this to academia.
2) Although the MAPT Roadmap focused on domestic needs, there should be a concerted outreach to the international community. What specifically can we learn from such models as Fraunhofer and IMEC as examples?
3) Due to the international nature of the semiconductor and advanced packaging there should be a concerted effort to try to work together with industry playing a key role in leading this effort. Prioritization should include how we address the global talent shortage, development of standards, and bringing the best thought leaders across the globe together to maximize impacts, and minimize redundancies including manufacturing, materials, sustainability etc.
4) Although only 3% of packaging and test is done here in the US, it will be difficult to bring those manufacturing operations back to the US however it is imperative that the US take a leadership role in advanced packaging to develop those technologies of the future. The US has a great opportunity to make this happen since the US leads in capabilities, including leveraging the National Labs, and academia which would allow us to leapfrog the traditional OSATs.
5) 3D Heterogenous Integration is a whole new ball game and represents the best opportunity to take a leadership role with limited investments due to a high need for automation.
6) Collaboration amongst all the stakeholder groups, both domestically and internationally is imperative. Government must also attempt to remove barriers to facilitate interagency interaction which can speed up technology maturation and introduction into the marketplace.
7) Shared accessibility, knowledge and collaboration is truly laudable and needed but questions around intellectual property will have to be answered beforehand to be truly embraced. An IP framework will be needed as we get to the maturity scale.
8) The MAPT Roadmap must address applications and demonstrations where there is a willingness to pay a very, very competitive salary to attract workers.
9) Environmental sustainability must be addressed including the circular priorities that will have a significant impact on supply chain.

10) The roadmap will primarily be used by both academic, labs and industry to help guide decision making in addressing research direction, funding priorities at both the federal and corporate level, training, and positioning relative to facilities and hiring etc.
11) Intellectual property concerns have stifled many good intentioned collaborations. It should be a priority, and given some real thought regarding how we can address, sooner than later.
12) This is a transformational and exciting time for our industry!