“Now What?”

Jim Wieser  - Aug 15, 2023
Director, University Research and Technology
CTO Office – Texas Instruments
Roadmap to Implementation → ACTION to Impact

Market-focused goals that support essential technology development, significant trends, applications, and the potential impacts of the five seismic shifts that are changing the future of Semiconductors and ICT.

**WHAT**

*Decadal Plan for Semiconductors Full Report*

January 2021

2030 Decadal Plan for Semiconductors

**HOW**

*MAPT*

March 2023

Microelectronics & Advanced Packaging Technologies (MAPT) Roadmap - Interim

**IMPLEMENTATION**

**Industry**

**Academia**

**SRC**

**DoC/DoD/DoE**

- NSTC
- NAPMP
- MMI
- ERI

Oct 2023+

Beyond MAPT
ACTION – *Execute to the Roadmap for Impact*

- Lead technology research and development
  - Industry + University + Government

- Facilitate research to manufacturing
  - Exploration through Prototyping and beyond

- Develop workforce pipeline
  - World-wide and nationally
  - Regionally – manufacturing sites
  - *Already seeing 40% increase in internships by semiconductor companies* *

- Maintain and further develop/update the roadmap
  - The industry is dynamic and MAPT needs to be a “living” document to be effective
    - Moore’s Law was an effective driver in the past and was quite focused
    - Future will be driven by applications and solutions rather than a specific technology
    - This will change over time as well as drive new technology needs
    - Identify gaps – current and future

* From Handshake July 25, 2023 event with US Secretary of Commerce Gina Raimondo
Impact – *leading indicators*?

- Use of the roadmap – industry, academia, government

- Awareness – the first step to impact
  - SRC Decadal Plan has generated notice and quoted in many presentations
    - University
    - Webinars
    - IMEC
    - ... and more

- MAPT Engagement
  - > 100 *participating organizations*
  - This conference

- Interim MAPT viewed by 5000+ views across 1700 users

https://srcmapt.org/
U.S. Competitiveness in a global industry

Challenges or Opportunities

Ref: Government Incentives and US Competitiveness in Semiconductor Manufacturing (SIA) - September 2020 – Antonio Varas, Raj Varadarajan, Jimmy Goodrich and Falan Yinug
What, When, How and WHO?
MAPT Roadmap Overview – many parts/complex
Complexity – Co-design and Coordination Key

- **Type 1: Late-stage prototyping, advanced nodes**
  - Users: <1nm transistors, next-gen memory
  - 300mm full flow, logic, memory, specialty
  - Now: commercial fabs; no open access
  - No/minimal changes allowed
  - Planar 28nm to 16nm FinFET, 1-nm and beyond
  - Buys access/incremental $ for 9902 annexes

- **Type 2: Mid-/late-stage prototyping, CMOS+X**
  - Users: MRAM+28nm, CIS, RF/MS, Emerging Memory
  - 300mm full flow CMOS + X logic or memory
  - Now: commercial fabs; no open access
  - Changes allowed, mostly in BEOL, some FEOL
  - Baseline CMOS (buy/make) FEOL+BEOL at 40nm/28nm & 16nm FinFET, 1-nm and beyond
  - Buys access/incremental $ for 9902 annexes

- **Type 3: Pathfinding**
  - Users: New mem, BEOL metal, process modules, heat spreading material
  - 300mm partial flow w/ integration
  - Now: ANT, IMEC, LETI, partial access
  - Changes and new materials allowed
  - NSTC module & process development
  - Runs partially finished wafers from Type 1 & 2 fabs
  - Buys access/incremental $ for 9902 annexes

- **Type 4: Mid-/late-stage pre-HVM, CMOS+X**
  - Users: Kepler, Ayar labs, GaN+CMOS
  - 200mm full flow CMOS+X
  - Now: SkyWater, Tower, MIT LL, Sandia, IMEC, LETI, HPI, GF, BTV, Xfab, partial access
  - New materials ok, mostly in BEOL, some FEOL
  - Runs partially finished wafers from foundries
  - Buys access/incremental $ for 9902 annexes

- **Type 5: Concept hardening to mid-stages**
  - Users: Gate stack, AlN/C, 2D, MEMS
  - 200mm partial flow w/ integration
  - Now: MIT LL, Sandia, IMEC, LETI, TSRL, partial access
  - Changes/new materials allowed
  - Runs partially finished wafers from foundries
  - Buys access/incremental $ for 9902 annexes

- **Type 6: NSTC-enhanced uniX facilities**
  - Users: 1,000 to 10,000-device demo, startups
  - Coupons, 100-200mm
  - Now: MIT, UCB, Cornell, Stanford, Purdue, ...
  - NSTC enhanced: staff operated, updated tools capabilities, duplicate tools for material compatibility, e-beam for fine litho
  - Runs wafers/coupons from foundries

- **Type 7a: Late-stage prototyping (coupled to Type 1,2,4)**
  - Users: Packaging houses, chiplet prototyping
  - Full flow (Advanced+standard packaging)
  - Now: commercial fabs (IBM, Bromont, Intel, TSMC, Amkor, ASE), no open access
  - No/minimal changes allowed
  - “Standard” chiplet interfaces
  - Potential sites for 9902 annexes

- **Type 7b: Pathfinding**
  - Users: Packaging materials suppliers, advanced packaging & system developers
  - Partial to Full flow w/flexibility w/HI
  - Now: IME, LETI, IMEC, Fraunhofer; not open
  - Capable of adv+standard packaging
  - Controlled changes allowed
  - Small volume, non-standard interface ok

- **Type 7c: Early-stage concept proof**
  - Users: advanced packaging researchers, tool suppliers, material suppliers
  - Coupons, die-level
  - Now: GaTech, SUNY Binghamton, UCLA...
  - Enhanced uniX labs; open access
  - Changes allowed; engineering staff to maintain tools and run processes
  - Site for process and tool development

June 6, 2023
Challenge – where to start, focus, prioritization

• Many interrelated parts of the industry
  • Coordination/collaboration will be key to success

• Heterogeneous/3D integration intensifies the interdependence of technologies
  • Materials
  • Devices
  • Design
  • Packaging
  • System
  • Test

• Impact
  • Where are the key gaps which make a difference?
  • What is already covered (by other programs) and may need a boost?
  • Where to NOT focus?
One Approach – IAC NSTC

- Identify the range of possible activities that might be carried out at proposed Technical Centers.
- Categorize activities by developmental stage, ranging from early research and pathfinding to late-stage prototyping, and by technology from the most advanced nodes to mature node and specialty technologies.
- Identify specific capabilities, associated physical assets, and baseline processes that should be supported and what level of access should be permitted.
- Identify examples of existing facilities that might be enhanced or used to fulfill the mission of the proposed Technical Centers.
- Examine a series of case studies for new technologies whose development might be carried out by NSTC Technical Centers.
- Test these case studies against the Technical Center capability map, trying to identify deficiencies.
Interagency Coordination

GOALS

1. Unified messaging on agency roles and responsibilities
2. Program coordination across agencies
3. IP and unique capability access across agencies
4. Fluid partnering with other agencies
5. Fluid partnering with federally funded institutions
Collaboration – govt agencies first step

Department of Commerce and Department of Defense Sign Memorandum of Agreement to Strengthen U.S. Defense Industrial Base

July 26, 2023

The United States Department of Commerce and Department of Defense have signed a Memorandum of Agreement to expand collaboration to strengthen the U.S. semiconductor defense industrial base. The agreement will increase information sharing between the Departments to facilitate close coordination on the CHIPS for America's incentives program, ensuring that their respective investments position the U.S. to produce semiconductor chips essential to national security and defense programs.
Learning – successes and programs

- **Common objectives to drive engagement and collaboration**
- University research groups
- SRC –
  - Industry
  - Govt
  - Academia
- Government
  - ERI
  - MMI
  - NIST
  - National labs
  - …
- SEMATECH
- Fraunhofer
- IMEC – successful research institute across industry, academia and government

Learn from Existing Programs
Learning Example – **IMEC key elements**

- **Sustainable** – since 1984
  - Government supported
  - Partners from companies, governments and academia

- **Global ecosystem** of more than 600 world-leading industry partners and a global academic network

- **Key facilities:**
  - **infrastructure** that includes a 2.5-billion-euro 300mm semiconductor **pilot line**

- **Expertise:**
  - CMOS: advanced & beyond
  - Sensing and actuation
  - Energy technologies
  - Integrated Photonics
  - Connectivity technology
  - GaN
  - Health technologies
  - Compute system arch.,
  - Artificial intelligence
Sustainable NSTC Model for US Semiconductor → Industry growth

Recommendation 4-2: The NSTC should develop a sustainable business model, with increased funding by industry over time. Government funding should provide risk capital to facilitate broad participation of firms and research institutions of all sizes and means.

- Industry and Government must **co-invest for the long term** to ensure sustainability and ongoing success.

**Considerations:**
- Successful PPPs strike a good balance between Industry and Government investment.
- Sustained government investment ensures **broad access** (start-ups, universities, small businesses) and increased **risk tolerance**.
- Sustained Industry investment ensures **relevance and evergreen capabilities**.
- Compared organizational models. IMEC, SRC, SEMATECH, etc.

Funding model based on insights provided by Dr. Paolo Gargioli.
Metrics – measure to improve towards impact

• Metrics drive awareness to move forward with impact

• Challenge is what to measure?
  • Technology improvement – incremental vs application impact
  • Application impact – application vs need
  • Social impact – need and quality of life
  • Leading indicators
    • Early awareness and planning
  • Lagging indicators
    • GDP
Summary

• **ACTION required for MAPT to have impact**
  - Metrics to track progress
  - Dynamic updating roadmap

• **MAPT – 3D / HI Microelectronics Roadmap**
  - Wide ranging
  - Complex

• **Coordination/Collaboration will facilitate**
  - Industry – implementation and workforce
  - Government – multiple agencies
  - Academia – research and workforce

• **Learning**
  - Sustainable, collaborative, infrastructure, expertise

• **Measure for Impact**
Thank You

Questions?
Session 7:

• **1:00 pm—2:30 pm**  
  **Executive Roundtable. MAPT Roadmap: Moving forward**

Now that the MAPT Roadmap is close to publication, we can more deeply engage in the discussions of: “What are the implications?” “How will we know whether we are progressing?” “What next?”

• **Keynote:**
  • Jim Wieser / Texas Instruments (CONFIRMED)
  • Title: MAPT to Coordinated ACTION and Impact

• **Panel / Open Mic Discussions**

• **Moderator:** George White (Georgia Tech)
  • Yuyun Shin / Samsung (CONFIRMED)
  • Krystyn Van Vliet / Cornell U. (CONFIRMED)
  • Ajit Manocha / SEMI (CONFIRMED)
  • Gabriela Cruz Thompson / Intel (CONFIRMED)
  • Gamal Refai-Ahmed / AMD (CONFIRMED)
  • Jay Lewis / NSTC (CONFIRMED)
Session 7: Panel Discussion Questions

1. We have a roadmap – now what?  Action but what action?  Who?
2. How do we use this roadmap to engage the international community?
3. Lots of discussion about advanced fab and packaging.  What action is needed to engage OSATs which are virtually 100% offshore today?
4. Semiconductor and microelectronics is a complex industry spanning from fundamental research to manufacturing billions of devices a year heading towards $1T/year aggregate revenues.
   1. Where should we focus for the biggest impact and “what” impact result?
   2. Where should we focus for the quickest impact and is this the right focus?
   3. What and how should we prioritize if we assume we can’t do it all – especially at once?

5. How much should government drive and/or fund the efforts to address the roadmap?
   1. NSTC and IAC indicates industry leadership but what does this mean?
   2. Who leads/coordinates/manages for best “national” success?
   3. Per question #3 – what is the metric(s) for success and leadership
      1. Total U.S. independence?
      2. Some % of independence?
   4. How much funding?  %?
   5. How long time frame?

6. What is really meant by the NSTC challenge for the U.S. to be leaders in semiconductor and what are the metrics?
   1. % manufacturing?
   2. % revenue?
   3. Most innovative processes, products, solutions towards real world application value?
   4. “Zero Footprint” environmental impact

7. The CHIPS initiative has been touted as being a collaborative effort between a number of federal agencies, which is necessary to ensure success. Can you tell us how you intend to leverage those best practices, and maybe cite some examples to ensure a successful outcome?

8. There is still some confusion regarding the roll out of the NAPMP.  Will its rollout coincide with the timeline for many of the semiconductor initiatives?