Abstract

Microelectronics and Advanced Packaging Technologies (MAPT) is a critical multidisciplinary field with the potential to transform the design and manufacture of future microchips. These advances build upon breakthroughs in advanced packaging, 3D monolithic and 2.5D/3D heterogeneous integration, electronic design automation, nanoscale manufacturing, and energy-efficient computing. The main goal of the conference is to unveil the Microelectronic and Advanced Packaging Technologies Roadmap – an industry-wide initiative of major impact on the semiconductor and ICT industry, which will drive public-private research investments in support of the CHIPS Act. The conference will celebrate the first 3D semiconductor roadmap to guide the forthcoming microelectronic revolution, like the International Technology Roadmap for Semiconductors (ITRS) has served in the past.

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MAPT Roadmap Conference  
August 14 & 15, 2023  
Holiday Inn Arlington at Ballston, 4610 Fairfax Dr, Arlington, VA

Technical Program

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<th>Day 1</th>
<th>August 14, 2023</th>
<th>Morning Sessions</th>
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<tr>
<td>7:30 am—8:15 am</td>
<td>Workshop Check-In</td>
<td>Ballroom, Lobby Level, Holiday Inn Arlington (all sessions will be held in this room)</td>
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| 8:15 am—8:45 am | Opening Plenary | Todd Younkin, President and CEO, SRC  
*The MAPT Roadmap - A Plan to Revitalize the Semiconductor Industry for Decades to Come* |
| 8:45 am—10:15 am | Session 1 | Advanced Packaging & Heterogeneous Integration  
(Session Chair: Muhannad Bakir / Georgia Tech) |
| Keynote | Griselda Bonilla / IBM  
*Accelerating HI Platforms to Enable Next Generation Systems* |
| Roundtable / Open Mic Discussions | See Discussion Questions on Page 5  
Charles Woychik / Skywater Technologies  
Henning Braunisch / Intel  
Shelby F. Nelson / Mosaic Microsystems  
Babu Mandava / 3D Glass Solutions  
George Orji / CHIPS R&D Office |
| 10:15 am—10:30 am | Break | |
| 10:30 am—12:00 pm | Session 2 | Microelectronics Workforce Development  
(Session Chair: Kashyap Yellai / SRC) |
| Keynote | Doreen Edwards / RIT  
*Talent Factories for chipmakers* |
| Roundtable / Open Mic Discussions | See Discussion Questions on Page 6  
Shari Liss / SEMI  
Shyam Aravamudhan / N.C. A&T State U  
Katy Crist / TEL  
John Goodenough / U Sheffield  
Quinn Spadola / NNCO |
| 12:00 pm—1:15 pm | Lunch | |
Day 1  August 14, 2023  Afternoon Sessions

1:15 pm—2:45 pm  Session 3  Sustainability and Energy Efficiency
(Session Chair: Jim Ang / PNNL)

Keynote  Brooke Tvermoes / IBM
MAPT Roadmap: Sustainability and Energy Efficiency

Roundtable / Open  See Discussion Questions on Page 7
Mic Discussions  Matt Marinella / Arizona State U
Katherine Hutchison / EMD Electronics
Sadas Shankar / SLAC National Laboratory
Austin Rovinski / NYU
David Speed / GlobalFoundries.

2:45 pm—3:00 pm  Break

3:00 pm—4:30 pm  Session 4  Foundational Microelectronics Layers of MAPT
(Session Chair: Kanad Ghose / Binghamton U)

Keynote  David Robertson / Analog Devices
Microelectronics Innovation in the Beyond Moore Era

Roundtable / Open  See Discussion Questions on Page 8
Mic Discussions  Tayseer Mahdi / Intel
Michael Spencer / Morgan State
Mary Ann Maher / Softmems
Thomas LeBrun / NIST
Min Tsao / Siemens EDA

4:30 pm  Conference Day 1 Concludes (followed by reception)
Day 2  August 15, 2023  Morning Sessions

8:30 am—10:00 am  Session 5  MAPT Systems: Specs, Applications and Security  
(Session Chair: Rafic Makki / Mubadala)

Keynote  
Ameen Akel/ Micron  
Applications, architectures, and systems of 2040

Roundtable / Open  
See Discussion Questions on Page 7
Mic Discussions  
Gamal Refai-Ahmed / AMD  
David Gundlach / NIST  
Farimah Farahmandi / U Florida  
Matt Klusas / Amazon

10:00 am—10:15 am  Break

10:15 am—11:45 am  Session 6  MAPT Ecosystem  
(Session Chair: Dave Henshall / SRC)

Keynote  
Katie Yu/ NXP  
MAPT: Ecosystem: Navigating Technology Economics For Market Growth

Roundtable / Open  
See Discussion Questions on Page 9
Mic Discussions  
Mitchell Heins / Synopsys  
Elisa Alonso / US Geol Survey  
Alain Diebold / SUNY Poly  
Kris Bertness / NIST  
Erik Hadland / SIA

11:45 am—1:00 pm  Lunch
**Day 2  August 15, 2023  Afternoon Sessions**

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<td><em>(Session Chair: George White / Georgia Tech)</em></td>
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<td>Yugyun Shin / Samsung</td>
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<td>Krystyn Van Vliet / Cornell U.</td>
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<td>Gabriela Cruz Thompson / Intel</td>
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<td>Gamal Refai-Ahmed / AMD</td>
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<td>Jay Lewis / NSTC</td>
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**2:30 pm—3:00 pm**  Closing Comments / Adjourn
Session 1 Discussion Questions

Keynote speakers and discussion panelists are asked to directly address the following questions in their remarks, to help the workshop sponsors better understand opportunities and challenges in each problem domain.

Session 1  Advanced Packaging & Heterogeneous Integration

This session focuses on various aspects of advanced packaging and heterogeneous integration of microelectronic chips. As the cost advantage of shrinking the die using finer transistor nodes (below 20nm) is diminishing, a new approach is necessary, which is to disaggregate a monolithic die into smaller chiplets cost-effectively fabricated on appropriate technology nodes. To enable functional scaling through heterogeneous integration (HI) of the chiplets and passive components, the package must transition from a chip carrier/encapsulation to an integration platform. The proliferation of chiplets will continue as industry drives towards higher performance lower power solutions that are customized for each application. The next generation of packaging technology needs to support this explosion in heterogeneous integration by enabling interconnects that accommodate very fine pitch I/O die and very fine lines/spaces circuitry.

Questions for the Panel:

1. Which are the packaging technologies that the US should focus on and how can we ever reclaim leadership in advanced packaging?
   i. What are barriers and what are the payoff in terms of the drivers (performance, energy, functionality etc)?
   ii. Will these technologies ensure we leap ahead everyone else?

2. 3DHI is application driven: sensing, communication, edge AI, data center etc. What are the challenges to integration of mm-wave, photonics, sensors, and high-voltage devices/chiplets in 3DHI and how will the technologies we just discussed help us here?

3. How can we better engage Universities to help solve challenges?
   i. Given the cost of the tools, space, and staff needed to have advanced HI research in academia, should we pursue central research nodes vs. distributing over a large number of schools
   ii. How can we create better pipelines from lab-to-fab in advanced packaging?

4. What are your thoughts regarding diversity, equity, and inclusion in the packaging arena and how do we improve it?

5. How long will the chiplet era last and what is life after chiplets?

6. Is an open chiplet ecosystem a pipe dream?

7. What are the opportunities & challenges for environmental sustainability with respect to packaging?
Session 2  Microelectronics Workforce Development

This session will discuss the MAPT workforce needs for the next decade. It is a national consensus that both the current talent pool and the pathways for creating and supporting a US domestic MAPT workforce fall far short of projected needs for the US and it has reached a critical point with respect to US economic and national security. The current pipeline for workers across the spectrum of education levels, from technical certifications, associate-degree operators and maintenance engineers to M.S. and Ph.D. engineers in microelectronics and advanced packaging technologies (MAPT), is insufficient in terms of numbers and of knowledge, skills, and abilities for tomorrow’s needs. This session will address: (i) projections/timeline for microelectronics workforce needs; (ii) roadmap for a nationwide “Winning Hearts and Minds” campaign; (iii) holistic, effective WFD framework for the entire MAPT eco-system.

Questions for the Panel:

1a. Who should “own” the semiconductor WFD “program”? Industry, Academia, Government. Assume ALL need to be active participants but without a lead/owner, there is risk of misdirected or fragmented efforts.
1b. If so, how should it be managed. - Centrally for the nation? Fully distributed to regions due to regional unique differences and needs.

2a. How can we incentivize the “missing millions” towards STEM from K-12 through to other sources and microelectronics when they probably are not even aware any opportunity exists?
2b. What is the BIGGEST challenge towards fulfilling the semiconductor workforce needs of the future? Is it Pure numbers, right skills, understanding the need – which skills and when, the right modeling and leverage of the model?

3a. There are many WFD and education programs, as we have seen in Chapter 7. How can we make these more effective, and what are the gaps? Do we need more?
3b. What is the biggest impact opportunity/approach we should prioritize to address the workforce shortage/needs of the industry?

4a. Is there a mismatch of new generation of student’s expectations and education/training needed to be effective for the semiconductor workforce? i.e., programming/coding has a very low barrier to entry while semiconductor design requires significant fundamentals and education – how can we best understand new generation student/workers and steer towards it?

5. Who is going to deliver the WFD program do we have enough inspirational educators and instructors to meet the needs? how do we encourage and incentivize a pipeline of educator talent?

6. This is a complex problem – where do we start/prioritize?
Session 3 Discussion Questions

Session 3  Sustainability and Energy Efficiency

This session will address the need for i) improvements in energy efficiency in computing, ii) increased environmental sustainability and efficiency across the entire lifecycle (e.g., design, development, manufacturing, use, end of life management) of semiconductor devices and systems, and iii) the development of the workforce needed to create new sustainable solutions and systems as societal needs change. According to the Decadal Plan for Semiconductors computing based on solutions we apply today are not sustainable now and will be impossible after 2040 as the energy requirements for that computing will outpace the energy available from the market as computing demand increases. Without 1000x improvement in energy efficiency in the next decade, and 1,000,000x improvement beyond 2040, computing will be in an energy-limited regime and will not grow, drive new markets, or spur global GDP growth. Also, as chip manufacturing in the United States is expected to increase in the coming years in response to the increasing global demand for semiconductors, and objectives of the CHIPS Act, it is imperative that the chemicals, materials, and processes involved in chip fabrication and advanced packaging as well as the product design itself are as sustainable as possible both from an environmental and human health standpoint.

Questions for the Panel:

1a. What energy efficient computing research areas are you most excited about?
1b. How can the industry best attain more energy efficient computing that bridges architectures and algorithms in addition to hardware and technology?
1c. What do you see as some of the most promising advances in advanced packaging technology and hardware that will improve the energy efficiency of computing?

2a. Energy efficiency of computing systems is often thought of in terms of energy per operation or performance per watt. Are these the most appropriate metrics to consider for energy efficiency?
2b. What are the best metrics to track sustainability and to understand the environmental impact of technology choices?

3a. What are the biggest challenges the industry faces with respect to reducing the overall environmental impact of semiconductor devices, materials and processes? What new solutions are needed to reduce the overall environmental impact of semiconductors?
3b. What does the industry need to focus on in the short-, medium- and long-term to decrease the environmental impact of semiconductors across their lifespan – from design, development, manufacturing, and end of life management?

4a. What are the economic incentives that will drive environmental sustainability performance, e.g. regulatory actions, establishing a carbon tax, or something else? How does the industry drive more focus on environmental sustainability and energy efficiency in semiconductor R&D? Are there examples of low hanging fruit?
4b. How does the industry drive better collaboration across the supply chain and semiconductor ecosystem to address these pressing environmental challenges?

5. How can chiplets and packaging improve the sustainability of semiconductor devices? Conversely, how can we develop chiplets, packaging designs and processes to ensure we avoid increasing sustainability challenges of semiconductors?
Session 4 Discussion Questions

**Session 4  Foundational Microelectronics Layers of MAPT**

The three foundational microelectronics layer of MAPT are: (i) Digital Processing, (ii) Analog and Mixed Signal Processing, and (iii) Photonics and MEMS.

Digital processing technologies have permeated into all aspects of our modern society. Processing costs are now dominated by the energy cost of moving data from their point of origin to the processing, and single chip-in-a-package solutions are no longer viable for addressing these data-intensive or high-performance processing needs. Heterogeneous integration (HI) of diverse unpackaged dies (chiplets) with a single package, resulting in a System-in-a-Package (SiP) has emerged as a solution to address these challenges.

Analog hardware is essential to world-machine interfaces, sensing, perception, communication, and reasoning systems, as well as the distribution, delivery and management of power to electrical systems of all types. Information from the physical world is analog and the exponentially increasing number sensors in the world are creating a large amount analog inputs where digitization of these signals would create a digital data load that would be near impossible to consume in downstream digital processors. Analog signals include the wired, wireless and optical communication, and we are also experiencing exponential growth in the number of communication nodes as well as the amount of data generated by each node.

Photonics and MEMS addresses important auxiliary technologies essential for memory, computing, sensing, communication etc. It is expected that photonics will play a critical role in driving innovations in the post Moore’s law era. Our evolving ICT culture will rely evermore heavily on photonics in collecting and moving the data. While integrated electronics may be approaching the physical limit, photonics integration has just begun. In the coming years, we will witness the exciting transition where the manufacturing processes of electronics and photonics are homogenized.

Questions for the Panel:

- **Is there life after CMOS?** What device technologies are practically viable (meaning, manufacturable and sold at scale) and should be pursued? What technologies are not worth exploring? Are spin-transistors one of the latter?
- **The energy challenge:** What new paradigms are required?
- **The future of memory and storage:** Memory devices are almost always analog even though they store bits. What do you see as the future of storing analog information in memory technologies that allow for in-place computing at the cell level?
- **Recurring rumors of an Analog Renaissance:** Recently, general-purpose analog computing has re-emerged as a viable alternative to digital computing that is significantly more energy efficient. However, isn’t it still plagued with the lack of reliability and consistency, particularly due to thermals and noise inside a package from nearby digital chiplets?
- **Is anything really digital?** The onion diagram in Session 4 keynote seems to imply that all interfaces are analog in nature, so this has to be case for a SiP. Yes, admittedly, analog signaling is used but the information they bear is digital. What is the solution for sending analog
signals/data AS SUCH across chiplets and between packages? Is this really possible? If this is not doable, aren’t we trying to overhype pure analog interfaces for chiplet-based solutions.

- **Power management and delivery:** It was noted that “Power is driven by the extremes”—what are the implications of that? Will single crystal GaN on GaN have any market impact? GaN or Si for in-package conversion, thermal co-design considerations? Associated HI challenges? What developments are needed for the passives to bring their form factor down for in-package applications with HI? Where will nanopower applications come from and how we power them. Role of energy harvesting, scavenging – at what point do we transition to this at nanoscale.

- **Do we need to talk about sensors as part of the semiconductor roadmap?** Isn’t this very different technology that should properly “sit outside the chip”?: Packaging challenges and co-design implications? Protection against damage to exposed parts? Test challenges for MEMS and how it affects overall testability. MEMS is just not another chiplet! Some in-situ processing inevitable → intelligent sensor.

- **Beyond conventional wafer processing (particularly for sensors):** Printed electronic devices?

- **Unique challenges for packaging HI sensors?**

- **Development Methodologies**—has complexity become intractable? Development costs are now so high that it seems that integrated solutions are out of reach for any application that does not sell 1BN units per year. How do we handle this?

**Heterogenous Integration and System Integration Topics**

- **The energy-efficiency challenge at scale:** Going beyond devices and interconnects for higher energy efficiency - HI is all about building systems on a chip. After all advances are made in devices and interconnects, what are the remaining knobs one can turn to improve the performance, energy-efficiency and scalability of the system?

- **Can the economic problem be solved?** It seems that we have a good idea of what HI is and how to put chiplets together. But challenges remain – what are the most important challenges that remain to be addressed for realizing digital SiPs and how do you rank them in from the most difficult to the least difficult? (Reliability, cost, testing, Co-design EDA etc.)

- **What will it take for the industry to truly move onto the “HI curve”?** We now have standards for chiplet interconnections and memory coherence. Do we need standards to facilitate chiplet stacking, such as for power and clock routing across layers?

- **Photonics interconnections** with package across chiplets – what’s the promise vs. ground-truth? Will these finally deliver?

- **Are we neglecting need of testability for HI at design, manufacturing and deployment phases:** (This can’t be an afterthought and has to be part of the integrated design process). The question of reliability in manufacturing looms large with HI systems, particularly with 3D HI. Are the test/run-time support being given any thought? In the interest of democratizing the HI industry-at-large, do we need to standardize these?
Session 5 Discussion Questions

Session 5  MAJT Systems: Specs, Applications and Security

ICT supports daily social life and economic activities. ICT has been and will continue to contribute greatly to the global economy. Applications are only limited by the processing power that can be delivered by today’s technology. While nobody can predict how ICT will develop in the future, it is worthwhile to explore best case scenarios that are bounded only by what is technically possible. This session will discuss the impacts of a wide variety of application domains and their influence on the direction of key enabling technologies covered by the MAJT roadmap, such as e.g. data center and HPC, mobile, automotive, biomedical, security and privacy, and others.

Questions for the Panel (highlighted questions are the top priority):

2040 Vision and Challenges
1) What are the major driving applications and systems envisioned for 2040, and why are we not well positioned to enable them?
2) How does the roadmap address the challenges for enabling these applications? What is the roadmap missing? What changes would you make and why?
3) What are some of the technologies likely to disrupt?

Enablement: Policies / Funding
1) Do we have the right policies in place to achieve the goals of the roadmap in terms of delivering on the application drivers? Do we need fundamentally new protections?
2) How can we best leverage application-focused efforts as part of the CHIPS Act?
3) Do we need a national systems/workloads collaboration center to tackle current and future bottlenecks? (e.g., memory systems, communications, etc.)
4) How do we get experts from different areas of focus to work together (e.g., security à applications à architectures à circuits à process)?
5) Applications implications on workforce development?

Application Drivers & Infrastructure
1) Are chiplets and HI enough? What additional efforts are necessary to enable continued systems/applications?
2) What about quantum computing?
3) Application driving path for manufacturing in the US
4) How do we best address developing the infrastructure for advanced packaging?

Security
1) Currently, performance is favored over security. Is there a future inflection point where the opposite becomes true?
2) Are there application domains where the opposite should be true?
3) What types of heterogeneity are relevant with respect to security? New security issues?
Session 6 Discussion Questions

Session 6  MAPT Ecosystem

MAPT Ecosystem includes i) Materials, Substrates, and Supply Chain, ii) Design, Modeling, Test and Standards, and iii) Manufacturing and Process Development Metrology. The discussion topics include identification of material and chemical needs used within future generations of advanced electronic package constructions, future design automation portfolios and development of industry standards, and the measurements that enable all aspects of semiconductor materials and device research, development, and manufacturing. This session will discuss the MAPT ecosystem and its foundational capabilities for all areas of the Microelectronics and Advanced Packaging Technology (MAPT) roadmap from materials and devices to advanced packaging and heterogeneous integration and systems.

Questions for the Panel:

1. What kinds of economic incentives can be provided to get various entities in the ecosystem to prioritize working on solutions to the identified gaps? This could be repeated for each of the three areas represented on the panel (e.g. Design, Materials and Metrology).

2. How can we start early in the engineering and R&D steps of MAPT to encourage the thinking/planning for resilient supply chains and to minimize dependence on critical minerals?

3. How do we ensure cost viability for on-shore mfg investments at all stages of the electronics supply chain?

4. What difficult challenges face metrology over the next 5 years? How have/can NIST and the National Labs accelerate metrology development? How to meet industry needs?

5. Can investments benefit HPC and industrial/automotive/consumer to protect economic sustainability/security?

6. Environmental Sustainability – How can we accelerate adoption? What are key challenges/needs? How might we accelerate the definition of a universal methodology with software enablement to measure carbon emissions and ecological footprint for both semiconductor and material suppliers through the full product life-cycle?

7. What issues such as the energy required for transportation should be considered outside the focus on the fab?

8. What types of investments are needed to fill in the gap between research and adoption?
Session 6 Discussion Questions

Session 7 Executive Roundtable. MAPT Roadmap: Moving forward

Now that the MAPT Roadmap is close to publication, we can more deeply engage in the discussions of: “What are the implications?” “How will we know whether we are progressing?” “What next?”

Questions for the Panel:

1. We have a roadmap – now what? Action but what action? Who?
2. How do we use this roadmap to engage the international community?
3. Lots of discussion about advanced fab and packaging. What action is needed to engage OSATs which are virtually 100% offshore today?
4. Semiconductor and microelectronics is a complex industry spanning from fundamental research to manufacturing billions of devices a year heading towards $1T/year aggregate revenues.
   a. Where should we focus for the biggest impact and “what” impact result?
   b. Where should we focus for the quickest impact and is this the right focus?
   c. What and how should we prioritize if we assume we can’t do it all – especially at once?
5. How much should government drive and/or fund the efforts to address the roadmap?
   a. NSTC and IAC indicates industry leadership but what does this mean?
   b. Who leads/coordinates/manages for best “national” success?
   c. Per question #3 – what is the metric(s) for success and leadership
      i. Total U.S. independence?
      ii. Some % of independence?
   d. How much funding? %?
   e. How long time frame?
6. What is really meant by the NSTC challenge for the U.S. to be leaders in semiconductor and what are the metrics? Leads: Gamal Ahmed (AMD), Jay Lewis (NSTC)
   a. % manufacturing?
   b. % revenue?
   c. Most innovative processes, products, solutions towards real world application value?
   d. “Zero Footprint” environmental impact
7. The CHIPS initiative has been touted as being a collaborative effort between a number of federal agencies, which is necessary to ensure success. Can you tell us how you intend to leverage those best practices, and maybe cite some examples to ensure a successful outcome?
8. There is still some confusion regarding the roll out of the NAPMP. Will its rollout coincide with the timeline for many of the semiconductor initiatives?
## MAPT Conference Attendees
### August 14th - 15th, 2023

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