Chapter 4
Design, Modeling, Test and Standards

4.1. Introduction

Designing, manufacturing, and deploying 3D heterogeneously integrated (3D-HI) systems-in-a-package (SiPs) that combine the strengths of best-in-class components will catalyze a new era of innovation for applications ranging from data center / HPC, to mobile / communications / infrastructures, edge / IoT, automotive, bio / health, defense / harsh environment, and others that may not yet be known to us.

An EDA portfolio that gives chip and system designers capabilities to explore and optimize across metrics of performance, power/energy, area/volume, reliability, security, and safety would be the key enabler for the semiconductor industry. A forward-looking view on EDA, demanding new ways of thinking about software architecture, algorithms, simulation/emulation hardware or cloud architecture, could also become an application driver for the very chips and hardware where EDA tools are run.

Defining such a roadmap, with both an “enabler” and a “driver” view, on a 5-15-year horizon, is the scope for the chapter.

The top three seismic EDA shifts we see are:

- System of chips (or chiplets) is the new SoC, and electronic-photonic-MEMS co-design is the new mixed-signal design paradigm (Figure 1).

- System-level full lifecycle robust design and optimization, from atoms, to devices, circuits, chiplets, chips, and hybrid interposers and from architecture exploration, to design, materials and process co-optimization, implementation, manufacturing, assembly and test, and deployment, assisted by AI/ML, provides new scaling drivers post Moore’s era (Figure 2).

- Among the observed trends, security of the design process, manufacturing process / supply chain, as well as the product itself is key to continue to reap benefits from an increasingly complex semiconductor ecosystem (Figure 3).
Table 4.1. Industry trends.

The MAPT roadmap recognizes that design and manufacturing are dependent upon each other and the more complex the system, the greater the opportunities for design and technology co-optimization (DTCO). This is especially true for multi-domain 3D-HI SiPs.

Key to design and manufacturing of advanced packaging-based 3D-HI SiPs are:

- agreed upon hardware architectures and interfaces including the package and interposers
- agreed upon manufacturing, assembly, and testing processes and associated design rules
- design automation tools and methodologies for co-design of multi-domain 3D-HI SiPs
- libraries of qualified and trusted building blocks (chiplets, interposers and packages)
- new material and multi-domain 3D-HI data models, simulation models, data formats, nomenclature, and data that include the package and interposers as part of the design as well as different forms of design parasitics (electrical, noise, thermal, loads, impedance etc.)
- methodologies and infrastructure to enable collaborative work across multi-company, multi-domain, geographically dispersed teams with shared data and resources

The industry has designed 3D-HI SiPs using standard 2D IC, board, and packaging CAD tools, but it required herculean efforts and employed mostly manual optimization and physical prototyping. More than four decades and hundreds of thousands of person-years have gone into the creation of design automation tools for electronic board and IC design. Similar, but more modest efforts have taken place for Packaging, MEMs, and Photonic ICs. Each of these efforts resulted in their own unique design methodologies, data
models, application programming interfaces (APIs), data formats, and nomenclature. Standards evolved during this time, but few if any data or interface standards exist for design flows comprehending packaging, 3D-HI SiPs, or co-design of multi-domain systems.

4.2. Multi-domain 3D SiP Design, Verification, & Test Methodologies

The industry needs to enable multi-domain 3D-HI SiP design capture, verification, and implementation using a diverse set of multi-domain chiplets assembled in a common package. The industry needs a plan to:

- reconcile and unify different domains’ (electronic, photonic, MEMS, mechanical) data and nomenclature
- establish version control methodologies in which one can envision large projects integrating multiple technologies, with each component moving through various revisions as multiple design teams work independently and asynchronously
- add new schemas that comprehend the aspects of different material systems, packaging, and connectivity (electrical, photonic, fluidic) used in 3D-HI SiPs,
- capture materials and assembly and manufacturing process constraints in the form of design rules that can be used by design automation tools to replace manual design, implementation, and verification steps
- investigate new tool architectures and data representations such as modular flat file interfaces that are programming-language and operating system neutral to remove potential barriers to software development; the industry should agree on standard description languages.

To achieve this, the industry will need to agree on several standards and methodologies. These include:

**Functional verification methodologies;** driving the types of modeling and data abstraction views required:

- CAD tool enhancements to include multi-domain co-design and analysis in 3D dimensions
- modeling for 3D mechanical assembly, stress, thermal, and bending that occurs during manufacturing and product use as this will drive 3D placement constraints of components
- modeling abstraction levels and how they are to be used in different combinations (stiction or ALD modeling, materials models up to software/hardware co-design).
- ensuring modeling abstractions are consistent and composable (FEM simulations consistent with SPICE for example) as well as models that are consistent and numerically well formed (modeling overpressure in microphones that cause SPICE simulations to glitch when simulating drive/sense loops)
- establishing standard verification IPs and protocols for acceptance testing of chiplets, and packaging data

**Hardware interface standards;** for combining multi-domain chiplets in a SiP such as the universal chiplet interface express (UCIe)

- electrical/optical interconnect fabrics and interfaces between mixed domain and mixed material chiplets, interposers, packages, and boards including analog as well as digital signaling
expanding upon concepts such as Networks-on-Chip (NoC) or Networks-on-Interposer (NoI) adopting new power distribution and thermal management methodologies for 3D-HI SiPs

**3D-HI SiP test methodologies;** for pre- and post-manufacturing and assembly:

- incorporation of multi-domain design-for-test methodologies that delaminate test strategies by domain including standard fault/failure modes, spec-based testing, etc.
- standardizing hardware design-for-test architectures including concepts such as built-in-self-test
- enabling controllability and observability through test architectures
- SiP failure mechanisms and data, along with test methods and scoring metrics for yield, assembly optimization, and system-level multi-domain testing
- methods for measuring and simulating chiplet, packaging, SiP, and system reliability and life cycles
- methods for securing and encrypting chiplet, package, and interposer test and debug data
- creation of commercial design tools to automate in-system sensor selection and placement with infrastructure automation to connect measured units to a processor with embedded software that is capable of making decisions about self-healing as a system ages
- methodologies and architectures to improve overall system reliability (self-checking and healing systems that make use of redundant interconnect and processing blocks)
- creating methodologies for testing of mechanical optical fiber alignment and accelerated life cycle testing to determine impacts of materials changes with temperature, aging, vibration, stress, and system activity

Finally, the industry needs to agree upon methodologies and methods needed for post-manufacturing tuning of SiPs, especially for systems containing analog/mixed signal, MEMs, and Photonics chiplets. Additionally, tools and methods to address post manufacturing flexibility enabling solutions to target multiple applications without new silicon chips.

**4.3. Automation and Collaborative Co-design**

Since chiplets in a SiP can themselves be systems-on-a-chip (SoCs), the complexity of a SiP can be considerable, representing Systems-of-Systems. The industry needs to research and employ advanced automation capabilities for collaborative co-design, optimization, assembly/implementation, and verification of these complex multi-domain 3D-HI SiPs.

The more complex the SiPs become the harder it is for designers to explore and trade-off different architectures that could be employed. As SiP design and verification methodologies become more mature and the industry solidifies on shared data models and schemas for representing multi-domain 3D systems the industry should shift focus to more advanced automation to include:

- 3D multi-domain co-design and implementation (including comprehending SiP assembly process and design rules - this has data implications for foundry and packaging design kits)
- adding enhanced parasitic extraction for the entire system, including the packaging and interposers used, that encompasses multiple energy domains – electronic, thermal, magnetic, photonic, and fluidic
- guided or automated 3D multi-domain architecture exploration and system partitioning with packaging included and comprehended as part of the system (this has implications on the data as relating to abstractions levels and models to be supported)
• synthesis and optimization as directed from constraints developed during architectural design
• use of Artificial Intelligence and Machine Learning type optimizations as appropriate to the tasks; research will also be needed to determine how to create models that can be used to train AI/ML

To enable multi-domain 3D-HI SiP designs, scalable collaborative design environments will be needed. Emerging designs will require disparate teams from different companies in geographically dispersed regions of the world to be able to work together and share access to chiplet and packaging IP from multiple suppliers. There is also a need to enable start-ups, small and medium sized entities, and educational institutions to be able to participate in the ecosystem. Emphasis should be placed on

• establishing, storing, and searching centralized libraries of chiplet-based functions for SiP design (this implies creation of a new ecosystem of suppliers and requirements for chiplet qualification and acceptance criteria)
• establishing, storing, and searching centralized libraries of packaging and interposer options for SiP design (this implies creation of a new ecosystem of suppliers and requirements for packaging qualification and acceptance criteria)
• standardizing chiplet and packaging IP-usage licensing terms and conditions
• development of cloud-based design environments that support multiple globally dispersed teams of different companies and disciplines working together using different abstraction levels of shared data
• enabling flexible cloud-based environments that offers scalability in both computational and capability resources, with pre-packaged design automation tools in a collaborative environment that ensures confidentiality.

Consortia such as SCALES need access to a streamlined, project-centric, cloud-based environments which reduce the cost of entry and ownership of design environments. A hosting organization could field requests from consortia members to allocate credits freeing members from establishing and maintaining costly hardware infrastructure, tools, licensing, and the specialized skills to maintain it. Such a design environment could be highly automated while also maintaining specialized flows for reuse. There is opportunity for automation in scheduling, with cloud-based environments offering the scale that no on-premises computing infrastructure could rival. Similarly, members that consent can contribute to building AI/ML models, significantly extending their lead.

4.4. Materials, 3D-Data and Data Standards

New materials will be key to driving innovations in manufacturing of multi-domain 3D-HI SiP devices to achieve needed performance and requirements for new applications. The incorporation of new materials into the manufacturing processes will require advances in modeling, simulation, and design tools. Important issues will be materials compatibility within a fabrication process sequence and whether proposed materials are allowable within a manufacturing facility. For example, some materials used in MEMS manufacturing are not compatible with IC manufacturing environments.

We envision new software, design and measurement tools will be needed to characterize materials in new ways for simulation including prediction under bending and stretching for flexible packaging used by wearables. Materials manufacturing compatibility design rules need to be created and incorporated into architectural trade-off, synthesis, and optimization design tools as well as those tools used by
manufacturing professionals. New tools are needed for ensuring performance of materials within expected environments such as fluids and biocompatibility for implantable systems.

In the longer term, tools are needed for materials optimization, engineering, and discovery to achieve desired properties by design. This will require design at the nano and atomic levels, cooperation between material scientists and manufacturing engineers, with new models and massive amounts of simulation driving a need for new compute power. Some tools exist in related fields but uptake within the semiconductor space has been slow.

Standards are required to enable interchange of materials and 3D-data between various entities involved in SiP design and manufacturing. Key drivers include the multiple physics field nature of the design and a need to design in 3D. Standards are needed for process / materials data exchange (types of data, units, how to measure key metrics). Standards will be needed to document behavior of materials in new ways as mentioned above under bending, stretching etc. It will also be important for manufacturers to quickly determine compliance with health and safety standards and requirements for proposed new materials.

Standards are needed for package provider data – libraries with relevant 3D data for design, assembly, analysis, and test. Some work has been done in this area with beginning work on packaging, but the work is far from over. A similar situation exists for chiplets. Standards are needed for chiplet provider data – libraries of electrical, photonic, and MEMs chiplets for SiP design. Standards are needed for SiP assembly & test data (Assembly Design Kit) – which includes 3D assembly design rules, and all 3D CAD views for the SiP design and implementation flows. As part of assembly, standards are needed for connectors that carry non-electrical signals such as fluidic signals. Finally, standards are needed for photonic and MEMS Process Design Kits- some PDK work has been done but the PDKs needed are more complex than IC PDKs as often wafer preparation information is needed and material properties in multiple energy domains must often be supplied.

A challenge in providing standards for manufacturing of HI devices is that there are often no standard fabrication processes as in the IC world and there are no standard primitives out of which devices are made. Fabrication of chips is highly application dependent or in the case of sensor chips based on the device physics used - magnetic, mechanical, optical etc. We do see some standardization in packages for certain types of devices, but we are far from a one size fits all world.

4.5. Security, Requirements Tracing and Life Cycle Management

With the establishment of 3D IC ecosystem, the business model will embrace globalization for lower cost shorter time-to-market. The supply chain and associated security issues are presented in the figure below.
Security

- **Chiplet security and trust**
  Designers of original component manufacturers (OCMs) create the hardware for chiplets and rely on offshore foundries to manufacture the chiplets. This can introduce security risks, such as IP piracy, as a rogue foundry, or foundry employee(s) may be able to extract high-level design information from the physical layouts.

- **Trojan threats and design theft**
  Trojan threats can originate from either the chiplet OCMs themselves, who may want to compromise other chiplets at the post-integration phase, or from untrusted foundries who may tamper with the physical designs or masks. As the chiplets flow through the complex supply chain, distributors or intermediate entities with advanced technical abilities can reverse engineer the chiplets to obtain design information such as layouts or netlists by studying the structure and transistors of the chiplets. This information can be valuable to competitors, as it can provide an illegitimate shortcut for costly research and development procedures. Additionally, counterfeit chiplets, such as those produced by rogue foundries or remarked items, may lead to unexpected failures if integrated into final 3D IC products due to potential defects, insufficient performance, and poor reliability.

- **Design for secure integration**
  Given the potential threats posed by chiplets and untrusted interposer layers from rogue foundries, 3D-IC SiP integrators often work to improve system-level security resilience by incorporating more design-for-secure integration components. In addition to chip-level security risks, inter-chiplet communication, which is facilitated by potentially untrusted interposer layers, is a major concern. Rogue foundries may cause information leakage through covert channels built on stealthy hardware Trojans in the interposers, or by implanting tiny wireless antennas on the interposer to create an information-bearing channel. They may also alter traffic on-the-fly to induce functional failures or intentional errors.
To address these issues, proper on-chip cryptographic infrastructure, such as encrypted communication between chiplets, should be used. Additionally, well-designed security policies need to be implemented and enforced in hardware to protect the confidentiality and integrity of sensitive information.

### Threat surfaces
Semi-invasive focused-ion beam (FIB) at the post-silicon phase can bypass hardware security features with minimal impact, requiring tamper detection measures like active shields. Additionally, many types of chiplets, such as CPUs and eFPGAs, rely on firmware stored in read-only memory to function. Attackers may tamper with the chiplet firmware through FIB or other physical attacks, providing a foothold into the infrastructure, evading detection at the operating system level, and disabling security features like secure boot or digital signatures to allow unauthorized software to run on the system stealthily.

In the in-field phase, adversarial end-users have access to the deployed systems, making physical attacks such as side-channel and fault injection possible ways to compromise the security of the system. Side-channel attacks use the physical characteristics like power consumption and electromagnetic emissions of a hardware implementation to extract sensitive information, such as the private key of a cryptographic engine. In the case of 3D ICs, the physical emissions may be more complex due to increased activity, but side-channel attacks can still be successful through advanced measurements and correlation of physical emissions with the correct key. Additionally, these attacks can occur within the system package, where a malicious chiplet can access the power supply of the target and analyze its fluctuations for malicious purposes.

Fault injection attacks are a physical method to compromise the integrity and confidentiality of security assets by causing glitches in the running implementation. These attacks can bypass built-in security mechanisms and deduce sensitive information through faulty outcomes, such as in the case of differential fault analysis (DFA) on AES. In a 3D IC, there are more security assets, making it more vulnerable to fault injection attacks than in a monolithic SoC scenario. Additionally, the varying technology nodes and speed of heterogeneous chiplets in a 3D IC increase the chances of successful fault injection. Furthermore, a malicious chiplet from an untrusted facility can draw a large amount of current to disrupt the power supply of its target, launching fault injection attacks inside the package, especially when power rail is not decoupled.

### Requirements Tracing
Many life-critical end-market applications such as systems in automobiles or medical equipment have strict requirement-tracing policies to ensure that specific requirements are built into the system from the beginning of the design process. These end-markets require methodologies and tools that can be used for

- Requirements capture
- Identifying the software and hardware system components that address each specific requirement
- Simulation to confirm specific requirements are met pre-manufacturing
- Testing, measuring, and analysis to ensure each requirement is met post-manufacturing
• Ensuring controllability and observability of all blocks fulfilling key requirements that are buried in the overall SiP

Lifecycle Management

The MAPT roadmap recognizes the need for extending design & manufacturing thinking to beyond time-zero, into full lifecycle of deployment, to detect and mitigate in-field variations.

Life cycle management of 3D chips involves:

• pre-manufacturing design verification and validation,
• post-manufacture testing and tuning and
• in-field performance monitoring and adaptation to electrical degradation.

Pre-manufacturing design verification and validation:

Future 3D-HI SiPs will integrate digital circuitry with multi-domain heterogeneous analog, RF, MEMs, and optics subsystems. While there are advanced tools for digital design verification and validation, the state of the art for mixed-signal circuits and systems is perhaps a decade behind corresponding tools for digital systems. New algorithms and techniques need to be developed for

• design verification and validation of 3D-HI SiPs and packages
• methods for applying existing digital verification techniques to digital-compatible representations of mixed-signal systems or developing new representations for analog performance in mixed signal systems
• use of optimized stimulus for stressing the performances of SiPs and packages, both pre- and post-manufacturing,
• techniques for diagnosing design bugs and correcting them to reduce the numbers of re-spins to reduce manufacturing costs.

To ensure the security of 3D IC devices during their prolonged in-field operations, it is essential to implement solutions that can protect against potential threats from untrusted components and external malicious intent. To maintain secure run-time operations throughout the device’s lifetime, embedded analog/digital sensors can be utilized to detect a wide range of anomalies caused by security vulnerabilities, such as sudden voltage drops or excessive thermal heat. These sensors can monitor these anomalies and trigger security policies to protect the device.

Post-manufacture testing and tuning:

Defect models for SiPs and packages need to be developed. Conventional catastrophic failure and timing-based defect models for digital circuits and systems need to be augmented with defect models for heterogeneous systems that include parametric as well as catastrophic defects in subsystems as well as interconnect and vias. Novel test stimulus generation algorithms are needed that can be used to test the performance of mixed-signal/mixed-technology components. This needs to be supported by appropriate design-for-test infrastructure for controllability and observability of embedded signals with minimal impact on device performance. Placing complex equipment such as spectrum analyzers on-chip for
performance assessment is impractical and expensive. Indirect, machine learning assisted test techniques are needed that allow monitoring of subsystem specifications without the use of on-chip specification measurement hardware. Finally, low-cost techniques are necessary for post-manufacture tuning of chip-package performances. Such tuning must be fast and allow maximal yield recovery even under large process excursions.

**In-field performance monitoring and adaptation to electrical degradation:**

Completely autonomous techniques that detect and correct both transient soft errors as well as performance deviations induced by electrical degradation and thermal effects are necessary for next-generation SiPs and packages. Thermal effects can cause significant performance degradation of advanced high-speed electronic systems and packages. On-line error detection techniques such as based on functional or algorithmic encodings of digital and mixed-signal systems may be used for this purpose. Error mitigation is achieved through judicious use of redundant computations (transient errors) or on-line tuning of circuit-level parameters (thermal effects/electrical degradation).

As 3D IC devices need to operate in the field for extended periods of time (typically over 10 years), some chiplets may need to be upgraded through remote firmware or software updates to address functional bugs and security vulnerabilities. If a secure channel is not available, man-in-the-middle or impersonation attacks may spoof software updates traffic by replacing it with malicious binaries. Ensuring the integrity of the supply chain is crucial for 3D IC devices as well since they are often expensive due to their high-power density and are thus at high risk of being counterfeited for profit. By implementing a zero-trust approach (e.g., blockchain-based tracking system) throughout the global supply chain, the threat of counterfeit 3D IC devices might be alleviated.

**4.6. State of the Art / Product Examples**

**Samsung High Bandwidth Memory (HBM)**
- **Significance:** First mainstream product using DRAM stacking
- **Limitation:** Cannot stack with logic chips due to thermal

**Intel Lakefield Processor**
- **Significance:** First mainstream product using heterogenous logic-on-logic stacking
- **Limitation:** DRAM is not directly stacked
4.7. Limitations with Current Technology

- Lack of industry standards in general limits the number of companies that can compete due to costs of having to reproduce base infrastructure
- Lack of industry design data and interoperability standards limits availability of CAD tools that can be used for design and verification
- Lack of industry repository for chiplets, interposers, and packaging IP makes it difficult for entities to search for building blocks that could lead to alternative, better solutions
- Lack of industry standard methodologies for chiplet specification and acceptance / validation testing makes it difficult for system engineers determine if available chiplets will meet their requirements.
- Lack of controlled and secure supply chain increase risk of rogue chiplets being used in mission critical systems
- General lack of design tools and design methodologies slows down innovation and sharing of IP building blocks (chiplets, interposers and packages)

4.8. Challenges, Future Needs and Possible solutions

Technical challenges are numerous and span from basic materials development to full system implementation and verification including architectural additions for improving system security and reliability. The most difficult challenge however is coming up with a way to marshal and organize the forces of a diverse ecosystem of companies who have different and many times opposing priorities and agendas for how to move forward. There needs to be a pulling force or goal that unites them to move in the same direction, much like the moon shots of the 1960’s.

Table 1 is a brief overview of the key areas of investment needed for 3D-HI SiP design.
Table 4. Key industry investment areas (Green – Process developed and ready for manufacturing, Yellow - Additional development work needed, and Red – Major development efforted needed for HVM)

<table>
<thead>
<tr>
<th>Investment Areas</th>
<th>Short Term (5 years)</th>
<th>Medium Term (10 years)</th>
<th>Long Term (15 years)</th>
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</table>
| Design Automation, Functional Verification, Physical Verification | • 3D-HI SiP design methodologies  
• 3D SIP assembly tools  
• 3D SIP simulation  
• SIP thermal analysis  
• SIP parasitic extraction  
• SIP DRC/LVS tools  
• Cloud-based design environments                | • Chiplet & Package version control  
• Advanced parasitic extraction for all design domains  
• Design/technology co-optimization                 | • Constraint driven 3D-HI SiP placement and routing  
                                                    |                                                                                       |                                                                                       | Architectural design exploration tools  
                                                    |                                                                                       |                                                                                       | Automated or directed AI/ML system synthesis |
| Materials, 3D-Data and Data Standards Data Interchange Hardware Architectures | • New materials characterization tools  
• New design rules for materials manufacturing compatibility  
• Reconcile data models  
• Reconcile modeling & abstractions  
• Inter-chiplet interfaces  
• Power distribution architectures  
• Standards for photonic and MEMs PDKs              | • Standardize nomenclature, and 3D-HI data models  
• Standards for process / materials data exchange  
• Tools for materials engineering, optimization, and discovery  
• Establish central chiplet, packaging, materials libraries  
• Massive parallel compute resources for materials simulation | • Network on Chip  
                                                    |                                                                                       |                                                                                       | Network on Interposer  
                                                    |                                                                                       |                                                                                       | Inter-chiplet photonic bus interfaces         |
| 3D-HI SiP Testing Design-for-Manufacturing Design-for-Test | • Test methodologies per domain (electronic, photonic, MEMs)  
• Post-manufacturing tuning methodologies            | • Chiplet & package acceptance testing  
• Standard failure models & metrics  
• Design-for-test architectures like scan, BIST, for each domain  
• In-package test structure synthesis  
• SIP manufacturing stochastic data modeling  
• Monte Carlo Analysis for yield prediction       | • Synthesis of SiP security architectures and protocols |
| Security Requirements Tracing Life-cycle Management | • Establish methodologies for creating secure SiPs  
• Facilitating trusted supply chains and security IP vendors  
• Establish SiP security scanning techniques  
• Establish SiP security standards and standard metrics | • Commercial SiP security scanning tools  
• In-system self-diagnostic security checking  
• Research SiP AI-based threat surface detection |                                                                                       |