Chapter 11
Analog and Mixed Signal Processing

11.1. Introduction

The recently published SRC Decadal Plan articulated several major challenges and seismic shifts with direct implications for analog/mixed signal semiconductor technology:

(#1) Fundamental breakthroughs in analog and mixed signal hardware are required to generate smarter, lower power world-machine interfaces that can sense, perceive and reason.

(#3) Always available communication requires new research directions that address the imbalance of communication capacity vs. data generation rates (including “6G” class wireless technologies)

Analog electronics deals with real-world continuously variable signals of multiple shapes. The analog electronics domain encompasses multiple dimensions, including: sensing, analog and digital/mixed signal processing, data conversion, communication, computation, power management, etc. Thus, the scope of the this chapter on Analog Processing includes (but is not limited to):

- Analog & Mixed-Signal circuits and processing
- Power conversion, management, and distribution (including high voltage/high current systems)
- RF-to-THz devices, circuits and systems

Each of these technical areas feature a number of different technologies that address numerous applications. This chapter is organized into subsections to address each of these major technology
areas, and we also refer the reader to Chapter 12, which addresses Optical, Photonics, MEMs and Sensor technologies, which are often intertwined with analog/mixed signal semiconductor issues.

For many of the above topics there is an integration imperative; while analog/mixed signal technologies often exploit more mature lithographies, it is frequently desirable to fabricate integrated circuits in a <55 nm node and use ultra-small and environment-proof packaging. Heterogenous integration technologies, including chiplets and 3-D integration techniques will have a significant impact in mixed signal products in the coming decade.

For high-frequency and high-power devices, new materials solutions need to be further developed. SiGe, InP, SiC and GaN devices are now being integrated at higher levels of hierarchy in ICs. New materials and device solutions such as AlN and Carbon-based electronics need to be included as future materials to be integrated.

New challenges arise to address the deluge of analog data in the RF to THz & Optical regimes, including devices, interconnect, power, dynamic range/ linearity, noise, time resolution/noise to packaging, antennas/interface, interference, and signal processing. It is important to optimize application-specific data rates for single-input-multiple-output (SIMO) and multiple-input-multiple-output (MIMO) systems (e.g. for automotive and industrial radars). It behooves designers to consider that low-level sensor fusion will require moving 10s-100s of Gbps of radar, camera, and lidar data to high performance fusion nodes in the near future, and that such high-traffic signal processing should be compatible with passive cooling and IC packaging.

For intelligent sensing, a key requirement to drive integration for size and weight, exploiting traditional and emerging monolithic technologies in addition to using board, flex, and package integration methods such as a triple-stacked sensor example (pixel+DRAM+logic) and various back-end monolithic or near monolithic integration technologies. New sensor modalities—including quantum sensing—need to be integrated at the system level. System co-design/co-optimization is necessary to satisfy the requirements stressing higher energy cost of data transfer versus processing.

There are numerous packaging and heterogeneous integration challenges: At THz frequencies, interfaces to the outside world are challenged by parasitic effects from traditional resistance, capacitance and inductance to fringing, roughness, and index of refraction at multi-GHz frequencies. The parasitic effects have severe effects on transmission loss and reflection impacting efficiency and signal-to-noise ratio. Additionally, integration of multiple technologies will be required and may not be possible on a single chip and/or require very closely couple passives. Large arrays in small form factors will challenge the pitch and likely require new 3-D solutions. In-package antenna technologies as well as exploitation of “meta-surface” technologies will likely be important.

Because analog/mixed signal ICs are often working at the interface with the physical world, many applications present special requirements with respect to extreme conditions. This may include temperature (extremes at both high temperature and cryogenic operation), voltage/current/power, exposure to radiation. In addition, posing special challenges for devices, these applications also may introduce demands for packaging, test, and EDA/simulation.

Architecture optimization covering device through interconnect and packing, plus coupling to the package, is a key area of research need.
Verification, production test (including known good die), metrology, quality, security, and failure analysis all present unique challenges in the sensor/analog/mixed signal domains. Significant breakthroughs and technology development will be required in these areas and are covered in detail in other chapters of this roadmap.

While analog/mixed signal (AMS) semiconductor systems share many fundamental characteristics with the digital/compute technologies that tend to drive a large share of the market and R&D spend, they also introduce some unique considerations, requiring special approaches to device and circuit design, system architecture and manufacturing. The AMS space is also exceptionally diverse, often requiring work across multiple technical domains. This suggests that issues like EDA, Security, Metrology, Packaging and Education/Workforce Development will need to comprehend AMS trends and challenges.
11.2 Analog Mixed-Signal Circuits and Processing

INTRODUCTION

The SRC Decadal Plan published in January 2021 outlines new trajectories for analog electronics. This chapter in the roadmap will summarize the short-, mid-, and long-term outlook for analog signal processing as it pertains to emerging applications and trends that are driving analog hardware. Analog component hardware is essential to world-machine interfaces, sensing, perception, and reasoning systems. Information from the physical world is analog and the exponentially increasing number sensors in the world are creating a large amount analog inputs where digitization of these signals would create a digital data load that would be near impossible to consume in downstream digital processors. Analog signal processing or processing at the “analog edge” can help mitigate the number of signals that must be processed digitally. In the following subsections we cover:

1. how analog and mixed-signal computation must scale to accommodate “analog edge” processing
2. the projected advancement of data converters necessary to accommodate larger bandwidths, higher throughputs, and finer resolutions
3. physical wireline and die-to-die interfaces; security; sensor fusion; clocking systems; and power mitigation techniques.

TECHNOLOGY SCALING AND APPLICATION DRIVERS

Among there many application drivers that require innovations in the analog / mixed-signal domain, the primary drivers include low-cost, energy-optimized intelligence across communication networks and compute, and high-throughput, low-latency, and high-bandwidth 6G wireless communication sensing, and high-performance data centers.

The performance and power-efficiency demands of the above emerging applications require drive towards 2.5D/3D architectures that bring challenges of cost, design methodologies, and thermal management. Technology scaling is heading towards sub-5nm nodes that incorporate gate-all-around transistors, nano-sheets, and fork-sheet based devices. Advanced packaging also plays an important role in shrinking large systems to nano-scale implementations.

In this section we review various aspects of analog and mixed-signal signal processing and how each is expected to advance in the next five to ten years. Each different area outlines how specifications and metrics are expected to advance over a ten-year period.
ANALOG AND MIXED-SIGNAL COMPUTATION

TRADITIONAL
Analog circuits in the next decade will evolve to make use of the many thousands of devices that can be dedicated to analog tasks. Analog design in prior years has depended upon the detailed performance of a few devices: the input stage of an amplifier, or the elements of the typical PLL circuit - these can be drawn as a schematic drawing and comprehended and improved by close scrutiny of individual devices behavior.

Over the next decade and into very small devices, this known art of analog design can be continued by series-parallel connections of multiple small devices, in effect using arrays of small devices to approximate the larger and better matched devices that the analog designer is familiar with.

However, as many thousands of small devices are employed the way they are connected need not be in simple series or parallel form. A new area of analog design can employ complex interconnections. As an example, the ubiquitous Gilbert Multiplier is a certain connection of six devices that creates a multiplier action; in advanced technologies tens of thousands of devices will be connected to create, for example, an FFT or voice activity detector and so forth. We are now beyond the schematic drawing era and entering a new possibly high-level language-based design framework that will enable these forms of analog design.

The Analog FFT is an example of a new analog methodology on an advanced process. In [1] and [2], demonstrations of the possibility of analog FFTs operating the analog domain with >12-bit, low-latency performance is enabled by tools and techniques that output tens of thousands devices with complex interconnection. Such designs are dominated by the artifacts of layout: inter-metal capacitances and so forth, and other parasitic effects that only become visible after layout is completed. Consequently, to achieve these new analog designs, CAD tools that can create prototype layout and allow the engineer to always have an estimate of the artifacts due to physical layout is necessary.

The new analog designer will work with layout as part of the design flow, which, with sufficiently sophisticated CAD tools, will be possible. However rather than considering the layout artifacts as a hindrance, they can be employed in the design to reduce power and increase accuracy. For example, in the design of an analog FFT processor two challenges must be met: the coefficient values in each analog neuron and the very complex connectivity to the next layer. The complex connectivity introduces track to track capacitances that degrade performance significantly. But a sufficiently sophisticated CAD tool can actually use these parasitic effects to create the required coefficients in the FFT. Thus, we are now in an era where the functionality of an analog device is not even apparent until the layout is complete. There are no parasitic effects - the layout artifacts are part of the design.

Much effort has been expended by the semiconductor fabrication providers on characterizing MOM capacitors. That will be extended to any arbitrary metallization such that above analog ideas are possible: the analog engineer is now using the layout artifacts (far beyond just a specific MOM structure) and so data on variability and so forth of arbitrary interconnect needs to be developed.

Analog signal processing blocks such as an analog FFT may impose new requirements on modules that interact with the analog signal processing blocks such as data converters. The traditional time division multiplexing of many analog-to-digital converters (ADCs) may be replaced with frequency division multiplexing. When this is done the requirement of the ADC is the rate of innovation of the signal, not
the arbitrarily high speed introduced by the time division multiplexing. In telecommunication systems
the rate of innovation in any given frequency of the ODFM is far less than the carrier or time-division
multiplexing action of current systems. Thus, power can be saved, and speed improved.

**OTHER ASPECTS OF ADVANCED NODES AND ANALOG SIGNAL PROCESSING: FINITE GATE CURRENT (TUNNELING CURRENT)**

In amplifiers of the current art certain base-current reduction techniques are employed. These are open
loop estimations of base current arranged by use of mirrors etc. to approximately cancel input current to
an amplifier. This methodology can be employed in advanced thin gate FET processes to do more than a
first order cancellation. Specifically, an entirely capacitively coupled continuous time signal chain can be
created where the DC operating point is controlled by a variable tunneling current at the amplifier inputs.
The advantage of this is that no noise is created by the signal path elements, and kT/C noise normally
present in a switch capacitor design is confined to a sub-band region of the signal. This is a technique in
use today in medical devices, but lower power and higher performance will result if the resistive FETS of
the known techniques are replaced with controlled gate tunneling current. This is another example
(similar to the inter-track capacitance mentioned above) where what may be considered an unhelpful
effect of advanced technology nodes may in fact improve performance.

![Figure 1. Analog Signal Processing in next five to ten years](image)

**EMERGING ANALOG SIGNAL PROCESSING**

In recent years, analog-in-memory computing for AI/ML has been seen in edge-based IoT systems due to
their energy-efficient operation. Bio-sensing and bio-computing based emerging components
necessitate analog processing due to the nanoscale nature of the compute or sensing action. Massive
MIMO array processing has seen optimum energy-efficiency operation when employing a hybrid
approach of processing across both the analog and digital domains, leveraging the best of each. Fully
Homomorphic encryption and implicit logic is a tremendous opportunity for analog computation, where analog computation is carried out without a DAC on the input and an ADC on the output, enabling implicit equation solutions (e.g., modulus of P/Q).

**NEAR ZERO-POWER PROCESSING**

Near-zero power processing is required for energy-harvested systems typically seen in bio-medical applications requiring lower power ADCs/DACs that can potentially be employed to encode the signal as a shift and scale invariant signal. Limited use of wires per signal and requirement of fast settling signals that are insensitive to first order single poles in the signal path are required. Increasing use of passives may also be required.

**TAKEAWAY AND SUMMARY**

The common theme emerging in analog / mixed-signal processing is that design must exploit analog processing opportunities as they arise and daringly move the traditional boundary between analog and digital to and moving the boundary to enable more processing in the analog signal domain when energy-efficiency or performance warrant such a decision.

**DATA CONVERTERS**

As described throughout the SRC Decadal Plan for Semiconductors, data converters (i.e., Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)) will play an increasingly critical role in a wide variety of applications ranging from intelligent sensing (e.g., using machine learning) for edge computing...
Meeting these levels of performance will require innovations in process technologies, application, and system-level architectures and in the data converter architectures themselves. Advances in process technologies often help since in most cases the transistors become faster as the geometries shrink, and some specific processes such as Fully Depleted Silicon-on-Insulator (FDSOI) and Silicon Germanium (SiGe) BiCMOS, that are more targeted towards analog/mixed-signal applications offer some significant advantages such as improved isolation and tightly controlled threshold voltages and high-speed bipolar transistors. However, in the case of CMOS technologies that are targeted at high-performance digital applications (e.g., 5nm CMOS), the supply voltages are consistently shrinking, and layout dependent effects (LDE) become more prevalent and actually make designing data converters with the required performance much more challenging. The drives the need for innovations at the system and data converter architecture levels going forward.

As shown in Figure 2, there is an extremely wide range of emerging applications that will require new and significantly improved data converter performance. As an example, consider the Analog and Mixed-Signal Computation techniques that are proposed earlier for more signal processing in the analog domain and data converter architectures for edge processing enable efficient and low latency sensing-to-analog-to-information as described in chapter 1 of the SRC Decadal Plan. Another example of an emerging application is accurately sensing low frequency/DC current signals in EV battery management applications where several hundred volts are used. Applications like this require specialized process technologies and architectures for the analog front ends.

In the mid-frequency range (e.g., 100KSPS to 500MSPS), applications ranging from high-fidelity digital audio to medical applications such as MRI and ultrasound to automotive applications such as motor control and safety (e.g., air bag control) will also require significantly improved performance (e.g., cost, power, accuracy, robustness, etc.) as volumes and required performance increase. Since many of these applications require high-accuracy, low-distortion performance in addition to being resistant to interference and especially reliable over a wide range of operating conditions, data converter architectures that meet these requirements with low cost and low power will become increasingly critical. Another example is ADC’s in car radio receivers that produce high-fidelity audio from the received signals. In this case, Spurious Free Dynamic Range (SFDR) is the critical specification. Requirements such as these become even more critical for medical and safety applications that can impact people’s health and quality of life. Possible new data converter architectures that could be applied to this application space include Artificial Intelligence (AI), Machine Learning (ML) assisted, time-based, hybrid SAR/pipelined ADCs, etc.

There is also an extremely wide range of emerging applications ranging from 5G/6G communications to high-speed serial links, to FMCW/PMCW automotive radars that require ultra-high speed, high-performance data converters of one kind or another. For example, for 6G small cell and Customer Premises Equipment (CPE) use cases, ADCs and DACs with ~10-b, 10Gs/s performance will be required. Given the significant amount of signal processing that is required for this application, the data converters must be implemented on the same SOC as the signal processing which raises the critical question of ‘partitioning’. In many cases, the continuously improving heterogeneous packaging capabilities enable critical IP to be developed in an optimal process technology for that IP and then be packaged along with other system components that have also been implemented in different but optimal process technologies.
to realize an optimal overall solution. But, as shown in the 6G small cell/CPE use case described above, there are also cases when critical data converters must be developed in a process technology that is definitely less than optimal.

Digitally Modulated Radar (DMR) (e.g., PMCW) for automotive radar use represents another example where the required digital signal processing demands that the data converters be integrated on the same die. So, on the one hand, ADCs and DACs that take best possible advantage of an optimized process technology (e.g., FDSOI or SiGe BiCMOS) with ultra-high-speed and resolution are needed, and on the other hand, ultra-high-speed and resolution ADCs and DACs are also needed in process technologies that are mainly intended for digital (e.g., 5nm CMOS). When an optimal process technology is available, fairly well-known architectures such as continuous-time sigma-delta or pipelined ADCs can be optimized to meet the application needs, but as application demands increase and especially when a non-optimal process technology must be used, new and innovative architectures must be developed.

Examples of emerging architectures for very high-speed applications include the continuous-time pipelined ADC that has been published by Analog Devices, ring-amplifier based architectures (e.g., pipelined ADCs) that have been published by researchers at Oregon State University and then IMEC, and also time-based ADC architectures such as those published by researchers at UC San Diego and Texas A&M University. Extensive research into optimal time-interleaving techniques is on-going and will need to continue into the future. It must also be noted that in the high-speed, high-performance application space, the need for correspondingly high-performance clocks is equally critical. For example, the 10-b, 10Gs/s ADC for 6G small cell/CPE use cases that is described above would require a clock at the ADC sampling circuit with ~40fs rms jitter which is obviously not a trivial requirement. This need will also drive close collaboration between data converter and clock IP developers.

For all of the applications/use cases described above, the overwhelmingly most important metric is whether or not the developed data converter actually works in the intended application over process, voltage, and temperature with high-yield and robust/safe long-term operation. As an example, in an FMCW radar transceiver, one of the most critical specifications is SFDR, since after processing, the received signals from targets show up as spurs in the ADC output and it is obviously critical that spurs generated by the ADC itself be significantly lower than the spur from any target. Once the data converter has been verified to work in the intended application, then other Figures of Merit (FOM) such as the Walden or Schreier FOMs can be used to compare performance.

For robust/safe operation improved simulation/analysis tools will be needed to meet the upcoming data converter needs that have been described above. For example, as described in Corner Models: Inaccurate at Best, and it Only Gets Worst ...by Colin McAndrew et al at IEEE CICC 2013, traditional PVT simulation techniques for analog/mixed-signal design are not accurate/adequate and robust statistical simulation techniques are needed. In addition, as the speed and resolution of the required data converters increases, and the used process technologies become ever more complex, simulations with the required accuracy become more and more difficult to complete and take longer. Another critical simulation requirement is the need to model and predict circuit behavior as devices age. So, enhanced simulation, modeling, and layout capabilities through collaboration between data converter designers and tool developers will also be needed.
DATA CONVERTERS FOR CELLULAR APPLICATIONS.
Cellular data converters can be roughly divided between base stations and user equipment (UE). In both cases there is a strong desire to cover the entire band with one ADC or DAC and this should be a focus of future research. For the ADC this typically means a bandwidth of several 100MHz and for the DAC about 4X-5X of this. The reason the DAC has to have more BW than the channel is that PA predistortion and/or envelope tracking is usually employed which necessitates a wider BW DAC.

The dynamic range requirements are medium hard, about 70-75dB / 100MHz carrier. Low power and low cost (= small area) are super important for all User equipment cases and also for base station data converters although to somewhat less extent. For the ADC converters the trend is moving towards RF sampling, meaning that the RF signal is sampled directly by the ADC.

As the radios are moving towards smaller and smaller nodes, the relative cost and area and power and speed of the digital logic improves compared the analog counter parts. Future research could look into how to leverage this power of digital to improve the data converters. One example is image cancellation inside the DAC to avoid expensive external filtering after the DAC and digital calibration of an ADC to make it better tolerate component mismatches, for example mismatches in SAR capacitor arrays.

In general, for a cellular ADC the key metric is not the SNDR, rather it is the ability of the ADC to process an in-band carrier in presence of an out-of-band jamming signal. Similarity for the DAC the objective is often to generate a good in-band signal while producing a minimum amount of out-of-band (i.e., RX band) noise.

SUMMARY AND KEY TAKEAWAY
Data converters with extremely wide range of performance will be needed in the coming years to address a wide range of system requirements for emerging applications. Data converters designed in digitally centric CMOS technologies below 5nm, will face more prevalent layout dependent effects (LDE) making high-performance data converter design more challenging, require more “digitization”, and will require innovations at the system and data converter architecture levels going forward. Systems for 6G will require high-resolution (>10-bit) and at least 10GS/s performance; given the significant amount of signal processing that will be required, data converters will need to be implemented in the same digital technologies and possibly even integrate some of the digital frontend signal processing tasks. It is expected that FoMs will be adjusted according to application imperatives.

WIRELINE PHY INTERFACES
Driving Applications: Networking, Storage, Automotive, High-Performance Computing and Accelerators
Key Performance Metrics: Data Rate [Gb/s], Reach (Insertion Loss) [dB], Power/Energy Efficiency [mW/Gb/s]/[pJ/bit], Bit Error Rate (BER), Modulation Type/Order.

Continually increasing aggregate bandwidth demands for networking and accelerator applications has led to a steep rise in required per lane data rates. Multiple wireline standards have announced per lane data rates beyond 50Gbps, with the highest currently at 224Gb/s. Following these trends, the per lane data rate appears to double every three to four years. To meet or even improve on these data rate projections
requires innovative solutions to issues including from I/O area and energy efficiency, circuit complexity, reliability, low jitter clock generation and distribution. While the high data rate drives the issues enumerated above, the solutions to each will be strongly influenced by channel loss at the specified data rate. As such, discussions of architectural and circuit choices are typically organized around the channel reach (a current stand-in for channel loss).

**LONG REACH**

Long reach applications are characterized by very high channel loss and unwieldy channel profiles. These features preclude simple linear equalizers in favor of high order, and sometimes nonlinear, equalization. Current realizations have converged on complex digital equalizers, requiring ultra-high-speed ADCs [3][4]. This choice requires innovations in both the mixed-signal frontend and digital equalization approaches to maintain area and energy efficiency. Highly interleaved data converters necessary to meet the required sampling rates (100GS/s to meet 200Gb/s/lane using PAM4) also drive the accuracy requirements of the clock generation and distribution blocks [5].

Looking to the future, a promising path is to make the advancements necessary in optical links to use such links in applications currently classified as long reach. Co-packaged optics [6], powered by continued form factor and cost reductions in photonics will enable the use of photonic links for long reach application. Minimal mixed-signal design techniques [7] in the interface circuits will ensure energy efficiency, even as the data rates are aggressively scaled. More importantly, mixed-signal design techniques could be refocused to resolving integration issues like degraded receiver sensitivity in co-packaged optics [8-9] or modulator nonidealities with PVT [12]. PDKs or modeling approaches [11] that enable this tight codesign and facilitate signal integrity and performance evaluation will be key to the success of this approach.

**MEDIUM/SHORT REACH**

The cost and form factor constraints may not support an optical solution for medium loss channel profiles. In these circumstances, a re-evaluation of the transceiver architecture away from the digital realization will clear the path for per lane data rate expansion. Innovative mixed-signal equalizers and low complexity digital equalizers may play a major role in keeping the energy efficiency high. New approaches centered around Correlative Channel Coding (or 1+αD) [12-19], Maximum Likelihood Sequence Estimation (MLSE) [18-19] and Deep Neural Network (DNN) [20-21] based equalizers, implemented in mixed-signal domain, will provide an alternative to ADC/DSP transceivers in high data rate applications. Folding in more traditional DSP techniques into the mixed-signal receiver will ensure improved energy efficiency, even as data rates are scaled.

**DIE-TO-DIE INTERCONNECTS**

This class of wireline links will benefit from all the innovations needed to aggressively expand the data rates of the longer reach variants. The data rate and reliability limitation here will have to do with the extent of advancement in packaging, peripheral component, and circuit scaling to fit I/O density constraints. Innovations to significantly reduce ESD size or develop a packaging approach that allows the
assembly and deployment of components with less protection will be needed. A redesign of the interface into a simpler RC interconnect that requires no termination will also be needed.

[May need to reference extra paragraph on 100GS/s data converters in data converters section ]

**SUMMARY AND KEY TAKEAWAYS**

*This section still under development*

**CLOCKING SYSTEMS**

- Clock Generation
- High-performance Applications
- Low-Power Applications

**SUMMARY AND KEY TAKEAWAYS**

*This section still under development*

**POWER MITIGATION TECHNIQUES**

- Power gating
- Clock gating
- Algorithmic techniques
- Near zero-power processing

**SUMMARY AND KEY TAKEAWAYS**

*This section still under development*

**SENSOR FUSION**

**SUMMARY AND KEY TAKEAWAYS**

*This section still under development*

**SECURITY, TRUST, AND RELIABILITY**

- Security, trust, and reliability for analog / mixed-signal systems

**SUMMARY AND KEY TAKEAWAYS**

*This section still under development*
CROSS-CUT: EDA TOOLS

MOTIVATION
As the performance, energy, and area demands placed on AMS circuits increase and as fabrication technologies advance, designers are navigating an increasingly complex design space to meet these needs.

- **Technology Scaling.** As we move to smaller process nodes and migrate to the deep nanoscale regime, it enables the development of ultra-high-frequency analog circuits. However, these smaller technology nodes experience larger mismatch (relative to device parameters), reduced gain, and exhibit a higher degree of sensitivity to circuit layout.[1] These challenges complicate circuit designs and leave little margin for error.

- **Application-Specific Circuits.** There has been significant interest in leveraging AMS systems for performing sensor processing tasks, performing computation in- and near-memory, and for enabling new forms of computation – these usages reduce data movement by performing computation directly on the signal of interest. A challenge to realizing these systems is identifying the right division of computation between the analog and digital processing elements, and settling on the optimal set of functional requirements, figures of merit, and design constraints to guide design.

- **New Fabrication and Device Technologies.** In recent years, an array of new device technologies and advanced integration processes have emerged that promise to deliver disruptive performance and energy benefits and enable new forms of computation. Because the design infrastructure for these technologies and our understanding of the associated physical processes is still evolving, architecting designs that use new devices is challenging.

If the cost of evaluating a design were free, this would radically change the design process. To design this next generation of AMS circuits, designers must carefully optimize the design, sizing, and layout of the circuit and efficiently navigate an increasingly complex tradeoff space to arrive at a good circuit design. Currently, it is prohibitively expensive for analog designers to effectively evaluate and optimize candidate designs due to the lack of automation. Very little of analog design today is truly automated in practice due to complexity of circuit dynamics that must be considered, lack of scalability of tooling, relative expense of accurate circuit simulation. Designers therefore have to expend a significant amount of manual effort to construct, optimize, and lay out potential circuit design – this high design cost significantly limits the space of circuits that can be explored.

It is therefore critical that we invest in next-generation AMS design productivity tools that enable designers to layout, explore, optimize, and validate analog designs at all levels of abstraction. These next-generation tools should enable designers to effectively explore the increasingly complex design space of technologies and process nodes to identify the best fit for their use-case.

**DESIGN SPECIFICATIONS**

Designers typically first elicit a behavioral description of the desired circuit (e.g., simulink model) and a
set of design requirements (e.g., gain & bandwidth requirements) from the client. This design elicitation process requires translating system-level design goals to circuit-level figures of merit.

**System-Level Design Goals.** Typically, the end-to-end metric to optimize (e.g., classification accuracy, inference time) is a complex system-level measure that requires evaluating the circuit in the context of the broader computing system.

**Figures of Merit for Circuits.** Analog designers typically optimize circuit-specific figures of merit – numerical measures that characterize the performance and properties of the circuit. The above system-level metrics need to be translated to design constraints over these figures of merit.

Negotiating the circuit’s design requirements is often productive, as reducing the complexity of the functional specification and relaxing the imposed design constraints can simplify the design of the circuit, and potentially enable designers to optimize for cost and resource utilization more aggressively.

In practice, negotiating these specifications is challenging because it requires communication with domain specialists who are often not circuit experts. Effectively communicating different design tradeoffs to non-specialists and incorporating specialist feedback requires navigating a not-insignificant communication gap between disciplines.

**Early Design Productivity Tools.** For these use cases, it would be productive to develop early design productivity tools (functional abstractions, early design exploration tools) to enable domain specialists and circuit experts to converge on a suitably flexible design specification that still achieves the system-level design goals. Digital designers have leveraged such co-design techniques to devise domain-specific accelerators that trade flexibility for performance.

**Simulation**
Analog circuit simulation is essential to evaluating the behavior of a circuit and understanding its performance characteristics. However, there is a fundamental tension between accurate simulation and computationally efficient simulation. This tension is exacerbated for circuits at smaller process nodes, as highly detailed physical models and advanced simulation processes (e.g., statistical simulation) are typically required to realistically evaluate a design. The usage of these more advanced models significantly increases the time required to simulate the design. Similarly performing simulations with the required accuracy becomes more and more time-intensive at higher frequencies and higher circuit complexities. So, enhanced simulation and modeling capabilities are needed to effectively evaluate this next generation of circuit designs.

**Circuit Design Optimization and Layout**
The analog design process involves architecting circuit designs, optimizing device parameters, and constructing circuit layouts that minimize resource usage and mitigate non-idealities. These steps of design affect one another – changing device parameters may require changes to the layout. In commercial design flows, circuit design and layout is manually done and parameter optimization is usually partially automated. Moreover, analog circuit designs are typically highly specialized to the process node, fabrication facility, and device technologies used and are therefore difficult to modularize and make portable. These factors make even small changes to a design costly and make it difficult to reuse designs. These issues are all exacerbated as technologies scale down and the physical effects of devices become
stronger. This lack of modularity and automation makes analog circuit design significantly more painful than digital circuit design.

Researchers have explored a range of techniques to expedite the design, optimization, and layout of analog circuits:

- **Analog Design Languages.** Recently, researchers have devised hardware generators that procedurally generate the design and layout for certain classes of circuits. [Berkeley, Berkeley analog generator] These generator-based design approaches require a significant amount of up-front work on the part of the analog designer but enable the development of reusable circuits that can be regenerated on-the-fly for different process nodes.

- **Automated Circuit Optimizers.** Researchers have also previously investigated push-button approaches that automatically perform parameter optimization and layout for a given circuit. These approaches leverage circuit simulation-based black-box and gray-box optimizers to evaluate parametrizations, and as a result, are time-intensive and have difficulties navigating larger optimization spaces. These performance issues arise because accurate circuit simulations are compute-intensive and black-box and gray-box optimizers take many iterations to converge.

Though some work has been done, there is a long way to go before we achieve fully automation optimization and layout of practical circuit designs. We recommend expanding on the above approaches and devising new design methodologies that are amenable to automation. In addition, more progress can potentially be made if this problem domain was made accessible to a broader set of people:

**Open Tool Flows.** This problem area would benefit from the continued development of scalable, open-source AMS design tools and open PDKs. These technologies facilitate workforce development, as individuals can contribute without requiring expensive licenses to proprietary CAD tools or special relationships with fabrication facilities. Efforts are already underway to develop open-source process design kits, low-cost tape outs (Global Foundries / Skywater), and open-source/free design tooling (CMC Electronics). These open tool flows may reduce hardware development costs, thus enabling analog designers to address the long tail of small/medium-scale application use-cases that can potentially benefit from AMS.

**Evaluation Metrics and Benchmark Sets.** In order to orient the broader community’s efforts toward solving problems that gate the design of commercial circuits and establish an evaluation standard, it would be productive to develop realistic, open-source analog circuit benchmarks for the community to use. Many fields, including digital design automation, use standard benchmark sets to systematically evaluate the efficacy of different approaches. A key question here would be, how does one evaluate if an automation technique that targets a large, open-source process node transfer well to an advanced, nanometer-scale process.

**Circuit Verification and Validation**

Analog verification & validation - Verilog-AMS, model checkers

- **Purpose:** finding system-level bugs in analog-digital design, validating analog design against functional specification. There have been high-profile bugs in analog components.
- **Challenges:** Typically this is done through exhaustive simulation against the Verilog-AMS model. This becomes impractical for complex designs that involve many analog and digital components.
- **Tie-in/ security**: brute-force testing not sufficient for protecting against adversaries.
- **Potential direction**: scalable analog validation to find design bugs early in design process.

### TABLE 11.2.1: TECHNOLOGY TIMELINE FOR ANALOG AND MIXED SIGNAL PROCESSING

*This item still under development*

### SUMMARY AND KEY TAKEAWAYS

*This section still under development*

### CROSS-CUT GROUP TOPICS

- EDA tools (data converters, analog signal processing)
  - Metrics are challenging and support in tools are limited
- Applications
- Packaging (wireline, radar)

### REFERENCES


11.3 Power Management, Power Distribution and Power Electronics

High Voltage/High Current Applications and Key Performance Parameters

Table 11.3.1 taken from the European Roadmap summarizes the applications and the driving metrics.

**Table 11.3.1:** Application areas for Power Electronics and drivers

As shown in the table, introduction of wide bandgap devices:

1) can increase the power reducing device volume and weight
2) can operate at high efficiency resulting in reduction of static losses
3) are highly rugged
4) have high temperature capability
5) are highly reliable.
Wide Bandgap Materials and Devices-

Over the last 10 years wide bandgap devices have emerged as alternate technologies for Silicon in many high voltage/ high current applications. The principal materials of commercial interest today are Silicon (Si), Silicon Carbide (SiC), and Gallium Nitride (GaN) which are often combined with alloys of Gallium Nitride and Aluminum Nitride (AlGaN). Currently SiC like Si is implemented as a vertical device on its own substrate while GaN is typically implement as a lateral device on a Si substrate. SiC devices are typically used in the highest voltage applications while GaN devices have a sweet spot of ≤650V applications. GaN device can be integrate with Si devices on the same die. For GaN to perform in high voltage applications vertical devices will need to be developed. While there are a few demonstrations of vertical GaN many issues with the technology remain.

- Ultimate breakdown voltage and device operating parameters for very high power
- Single device vs series parallel combination
- GaN on Si versus GaN on GaN
- Ga₂O₃

Key challenges moving forward are:

1. Continuing to address the device reliability and ruggedness. Issues include the short circuit avalanche performance and development of the JEDEC specification for wide bandgap devices.
2. Development of fully integrated GaN power electronic devices. Current GaN power devices exist as hybrids with Si technology. Moving forward the challenges on system on a chip (gate drivers and real time diagnostics) need to be addressed with the goal of eliminating inductances.
3. GaN materials technology presents many challenges to implementation of a vertical device technology. Among these are 1) development of a low cost, low defect, large area substrate. 2) continued development of ion implantation and annealing technology and 3) better edge terminations for devices.
4. SiC materials technology despite its relative maturity still limits usable device area because of substrates defects such as threading screw dislocations and basal plane dislocations. Further gate oxide for MOS devices still presents challenges.

Power circuit architecture

Key Issues

1. Trade off between conversion ratio and efficiency
2. Interconnect at different levels of power
3. Vertical power delivery
4. Better device models for wide bandgaps
5. Data center currently converts between 48 and 12 V Can we go below 12 V

Nano Power

Nano power is becoming more and more prevalent. Key applications include the Internet of Things (IOT) and wearable applications addressing personal medical data collections. In the medical space data
collection is currently centered around cardiology but we anticipate monitoring physio-chemistry use blood, sweat, and saliva. Most applications use lithium ions batteries instead of energy harvesting. These applications often require a wide dynamic range of power and a high efficiency through this dynamic range.

Key Issues

1. Optimization of size and cost.
2. Form factor
3. Inductor-less power
4. Future types of power may include biofuel cells
5. Good power efficiency through the dynamic range
6. Large load steps such as going from nano amps to milli amps quickly requires a good controller to respond quickly

Energy Storage Elements

Energy storage/passive elements are a critical part of power conversion circuitry—whether integrated monolithically, as part of a module, or external. Technical advances in these components (in size/density, ability to handle higher voltages/currents/thermal conditions) can have a significant impact on power management/distribution systems.

- Capacitors
- Inductors
- Piezoelectric

**Table 11.3.2: Technology Timeline for Power Management and Distribution**

*This item still under development*
11.4 RF to THz Devices, Circuits and Systems

Purpose

In defining a decadal plan to develop underlying technologies (IC technologies, interposers, packages, etc.) for wireless systems, we must first project what type of systems will likely be developed in the next decade. Yet, the type of systems deployed depends not only on technical factors but also on wireless communications market growth, on deployment costs, and on the level of propagation losses arising from partial or complete beam blockage. Many of these factors are outside the expertise of the primarily semiconductor and circuit experts on the wireless roadmap committee. We therefore seek to list some of the emerging technologies and factors that might cause these to succeed or fail in commercial deployment.

Applications, Frequency Bands, and Wireless equipment

The applications include automotive radar, mobile wireless endpoint, i.e. delivery of signals to the mobile end user, and fixed wireless endpoint, i.e. delivery of data to fixed locations such as homes and businesses. These both communicate to the wireless end user equipment with wireless hubs; the hub can be connected to the main network either with optical fibers or with wireless backhaul. When the hubs are closely spaced, the backhaul links will have shorter range and perhaps lower data capacity: this is called wireless fronthaul. Such links need fronthaul and backhaul transceivers.

The frequency bands\(^1\) for these, now or in the future include sub-6 GHz, 28 GHz, and 39 GHz, these part of present 5G hardware. Other frequency bands, either already allocated for wireless communications and/or radar, or of interest, include ~75-85 GHz, ~90-95 GHz, ~135-175 GHz, and 210-310 GHz.

Choice of Frequency Band: Principles

In automotive radar, shorter wavelengths provide better angular resolution for given radar antenna array area. Improved angular resolution allows better discrimination of important adjacent objects, e.g. a motorcyclist stopped under a bridge, or some pedestrians standing beside a roadway but others standing on it. Higher carrier frequencies are therefore desirable if the ICs and packages work well and cost little. Although increasing the carrier frequency increases the worst-case atmospheric attenuation, automotive radar need not work over very long range. For example, when a car travels at 67 MPH, a 300 meter range radar will provide 10 seconds warning of a hazard. Given such short range, even the attenuation from extreme rain can be accommodated; further, radar range can be allowed to

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\(^1\) I am only passingly familiar with the exact FCC frequency allocations. The MAPT document must be checked by someone who knows these well. There's some information at https://en.wikipedia.org/wiki/5G_NR_frequency_bands, others at https://halberdbastion.com/technology/cellular/5g-nr/5g-frequency-bands
decrease in extreme rain, as a car cannot be safely controlled if driven at 67 MPH in extreme rain, even if the radar lets the driver see ahead.

Higher carrier frequencies also make MIMO systems smaller, hence easier to deploy. MIMO systems use many antennas to radiate multiple independent signal beams, each carrying separate data. The radio spectrum is re-used many times, supporting a larger capacity in a given allocated bandwidth. In MIMO hubs, the array width varies as the inverse of frequency. In MIMO backhaul and endpoint links, the MIMO array length varies as the inverse square root of frequency; higher frequencies make high-capacity MIMO systems more compact and therefore more practical.

In wireless communications, governments will likely allocate more spectrum at higher frequencies because there is more spectrum available there. The wider the allocated spectrum, the greater the feasible data transmission rate at a given power efficiency: more complex modulation permits faster data transmission in a given bandwidth, but the power we must radiate to do this increases exponentially.

Disadvantages for high-frequency systems include higher cost and poorer performance of the transmitter and receiver ICs, increased worst-case atmospheric attenuation reducing range, greater probability of beam blockage from objects lying between the transmitter and receiver, including foliage and trees.

Given greater atmospheric attenuation, high-frequency systems generally support shorter propagation ranges. Water vapor attenuation in hot, humid weather becomes extreme above 300 GHz. Systems operating above 300 GHz must either be extremely short range, must avoid places in the world where there is hot, humid weather, or must operate at higher altitudes, avoiding the air and its moisture.

High-frequency wireless signals are more easily blocked. At a distance $R$ from a receiver, an object of area $\sim \lambda R$, the 1st Fresnel zone area, will block most of the power. Such blockage can occur with discrete objects, or from the collective effects of many small ones, e.g. beam blockage due to leaves on a tree. High frequency signals are more easily blocked.

**Choice of carrier frequency for automotive radar**

Given that automotive radar need not support extremely long range, increased atmospheric attenuation is not a substantial disadvantage. Higher-frequency systems offer better angular resolution, but ICs and packages perform less well (and/or are more expensive). 75 GHz band automotive radar is widely sold today. 140 GHz automotive radar is readily feasible in low-cost production CMOS and high-volume SiGe BiCMOS technologies; approximately 200 GHz appears to be the upper limit of low-cost mass-market IC technologies today.

Given the potential for further improved angular resolution, automotive radar systems above 200 GHz, perhaps as high as 300 GHz, may be of commercial interest. This will require use of semiconductor technologies having higher power-gain cutoff frequencies (500-600 GHz) than the ~300 GHz of current high-volume CMOS and SiGe BiCMOS technologies. Power gain cutoff frequencies of 700 GHz (SiGe HBT), 1100 GHz (InP HBT) and 1500 GHz (InP HEMT) have been demonstrated in low-volume laboratory and/or pilot line processes. Mass production of automotive radar systems above 200 GHz would
require bringing one of these materials into high-volume, high-yield, low-cost manufacturing. Heterogeneous integration technologies could be a favorable solution because it would permit such transceivers to be constructed using only very small dies of the advanced high-frequency ICs, with the vast majority of the IC area in VLSI CMOS.

**Choice of carrier frequency for wireless communications**

With the advent of 5G systems, cell phone handsets with 28 GHz and 39 GHz transceivers are available to the public. Yet, during 2020-2022, worldwide adoption of such hardware has been slow. This may simply reflect slow development of high-capacity wireless markets. It may also reflect fundamental difficulties with high-frequency propagation. The roadmap must acknowledge this uncertainty.

**Mobile wireless endpoint** connects the hub to the cell phone handset. The path of such links varies greatly as users move, hence path loss from blockage is likely. This is the application where the high path losses and high blockage probabilities of high-frequency systems pose the greatest difficulty. Though commercial deployment of 28 GHz and 39 GHz systems is ongoing, it’s possible that future mobile wireless endpoint links may migrate to lower frequencies, between the present sub-6 GHz and 28 GHz bands, to minimize path losses and beam blockage probability. To provide the needed capacity with lower carrier frequencies, hence lower bandwidth, massive MIMO will be required. Thus, one path for mobile wireless endpoint in the next decade is microwave massive MIMO. On the other hand, slow 28 GHz and 39 GHz adoption may simply reflect slow growth of the wireless data transmission market. If so, as capacity at 28 GHz and 39 GHz is exhausted, in the next decade mobile wireless endpoint may migrate to 70-75 GHz, and even possibly 135-145 GHz.

For mobile endpoint, the choice of carrier frequency strongly depends on market growth. If the information density (Gb/s/km²) is low, wireless hubs should be widely spaced to keep infrastructure costs low. If the information density is high, cellular areas, hence hub spacings, will be reduced to reduce the total data capacity per hub. The propagation distance between hub and user then becomes smaller, and the high atmospheric attenuation and the greater probability of beam blockage become less serious limitations of high-frequency systems.

**Wireless backhaul and fronthaul** connect hubs to the internet backbone. Lower-frequency systems provide greater range; higher-frequency systems can provide greater capacity, both from more available spectrum and from being able to support MIMO in an array of smaller dimensions. Given the frequency dependence of rain attenuation noted above, systems providing more than 1 km range will, in the next decade, most likely use <35 GHz carrier frequencies, with range increasing as the frequency decreases; feasible data rates are then c.a. 10Gb/s or less. Systems at 75, 140, 210, or even 280 GHz can support 100-1000 Gb/s data rates, but >700 m range will be difficult to support. Beam blockage is less problematic in such systems, as the propagation path is known. **Fixed wireless endpoint** will use hardware and deployments similar to fronthaul, but the needed capacity per endpoint links will be smaller than that of backhaul. Carrier frequencies at 28, 39, 75, and perhaps even 140 GHz are feasible; even the 75 GHz band should be sufficient to provide >50 Gb/s/link, sufficient for the next decade for many fixed destinations.
IC technologies

RF-optimized mass production CMOS VLSI technologies today provide 300 GHz power-gain cutoff frequencies. CMOS transistor noise figure and CMOS transistor RF output power is sufficient to support high-performance RF/wireless mobile transceivers below 100 GHz. For hub and backhaul transceivers operating below 100 GHz, the CMOS chip set may be supplemented with GaN HEMT or SiGe HBT power amplifiers. Between 100-160 GHz, CMOS IC performance is sufficient to shorter-range links. Combining CMOS with a InP HBT, SiGe HBT, or GaN HEMT power amplifier or with an InP HEMT low-noise amplifier will permit links of greater range or higher capacity.

Mass production SiGe BiCMOS have cutoff frequencies similar to CMOS, but higher performance SiGe HBTs have been reported as laboratory demonstrations or as pilot production technologies. As these transition to mass production, higher-frequency systems will become feasible in Si technologies.

InP HBT technology, today established in low-volume pilot production, readily enables 100-300 GHz power amplifiers of record power and efficiency. If the market demand can support the cost of doing so, production versions of InP HBT technology might emerge.

InP HEMT technology, today established in low-volume pilot production for military and scientific applications, is by far the lowest noise figure transistor technology at any frequency. If the market demand can support the cost of doing so, production versions of InP HEMT technology might emerge.

Below 100 GHz, GaN HEMT technology provides record RF output power and efficiency. There are R&D efforts worldwide to extend and improve the performance of GaN HEMT as an efficient power technology above 100 GHz.

Package Technologies

IC-interposer interfaces using flip-chip bonds with Cu studs have been developed for connecting microprocessors to memory and other digital ICs. The high-density Cu-stud flip-chip technology performs well even over DC-300 GHz. This therefore provides an excellent baseline package technology for wireless systems.

Packages for wireless systems, particularly at 30-300 GHz, to support efficient antennas and low-loss transmission lines, also require at least one plane of low-dielectric-constant materials. The package's dielectric materials must have either high thermal conductivity to support heat removal from ICs and power amplifier transistors or must provide dense arrays of thermal vias for heat removal. Generally, the package must simultaneously support high densities, low dielectric constants, and high thermal conductivity.

In the next decade, many wireless systems will integrate CMOS transmitter and receiver ICs closely integrated with very small-scale non-CMOS (SiGe HBT, InP HBT, InP HEMT, GaN HEMT) power amplifier and low-noise amplifier ICs. The package must support dense integration of these, adequate thermal management, and appropriate high-frequency connections. Package design is made more difficult in higher-frequency arrays, where RF channels and antennas must often be placed at a half-wavelength lateral (horizontal) pitch. In fixed-infrastructure transceivers such as those used for hubs and fronthaul and backhaul transceivers, the required range of vertical beamsteering is considerably less than 180 degrees, hence though the array element lateral pitch may be constrained to half-wavelength, the array
element vertical pitch may be several wavelengths. With larger area available per RF channel, demands on package integration density and thermal density are somewhat relaxed.

**Special Technologies: Antennas, Meta-Surfaces, etc**

*This section still under development*

**Related Technologies: Radio processors**

Signal processing of large array systems with GHz bandwidth and low latency requirements creates some unique and extreme processing demands. In many cases, these processors may need to be optimized for their requirements and may be distinct from the processors required for conventional high performance computing or even GPU/AI workloads. We will reference the work of Chapter 10, but will also track the particular developments for these high performance GHz bandwidth systems.

**TABLE 11.4.1: TECHNOLOGY TIMELINE FOR RF/THz CIRCUITS AND SYSTEMS**

*This item still under development*